

Fig. 1 Prior Art

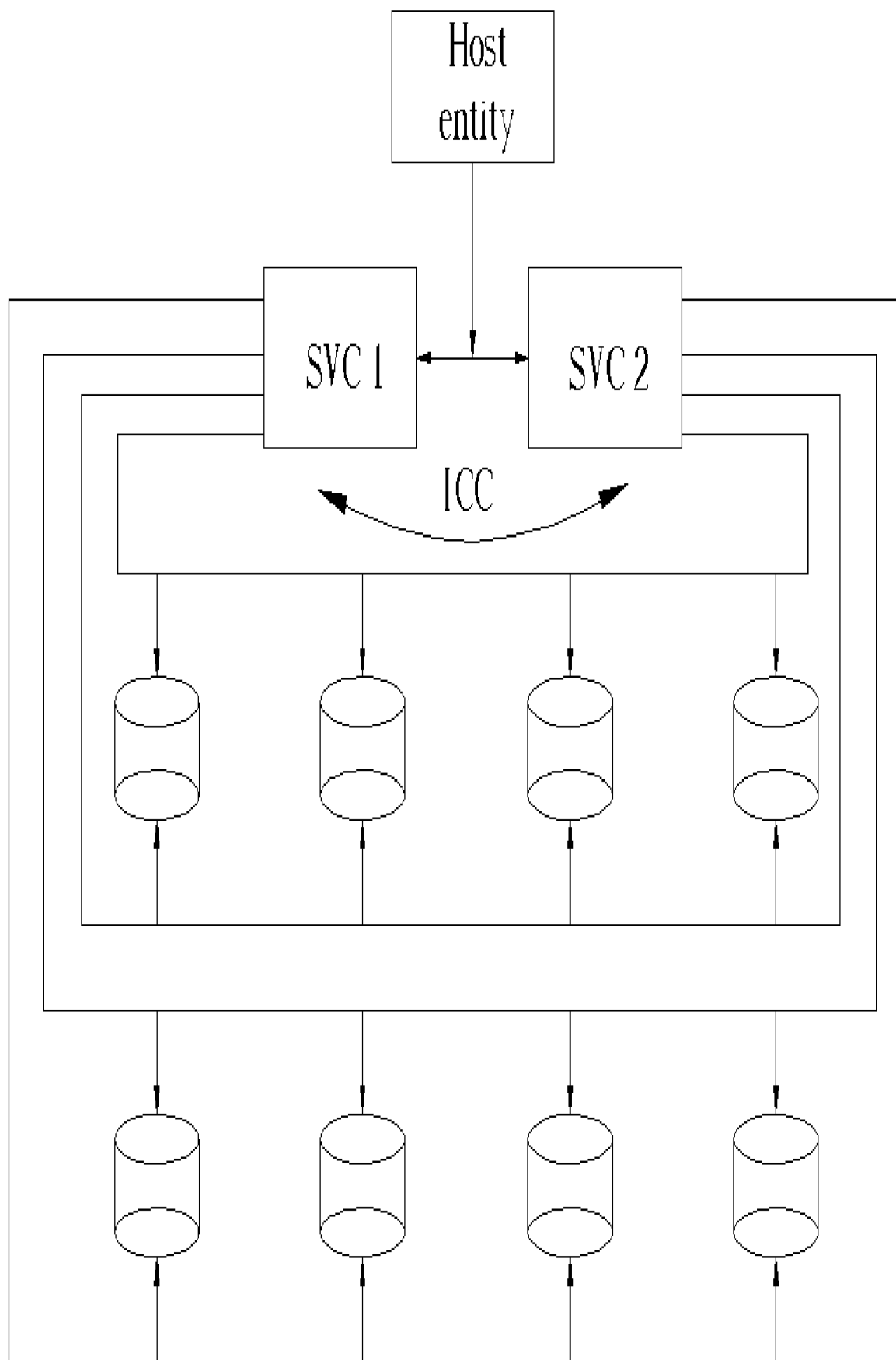


Fig. 2 Prior Art

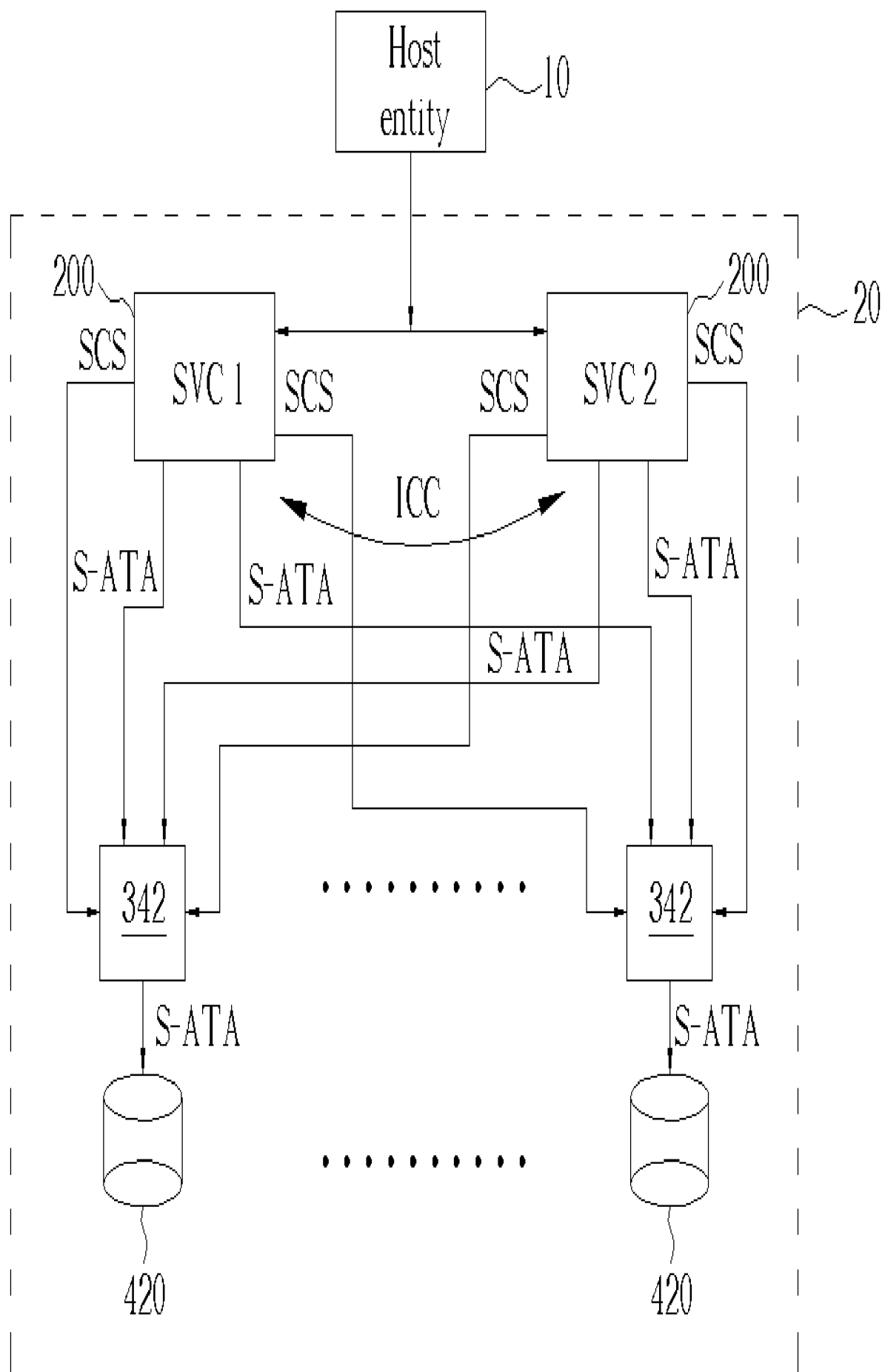


Fig. 3

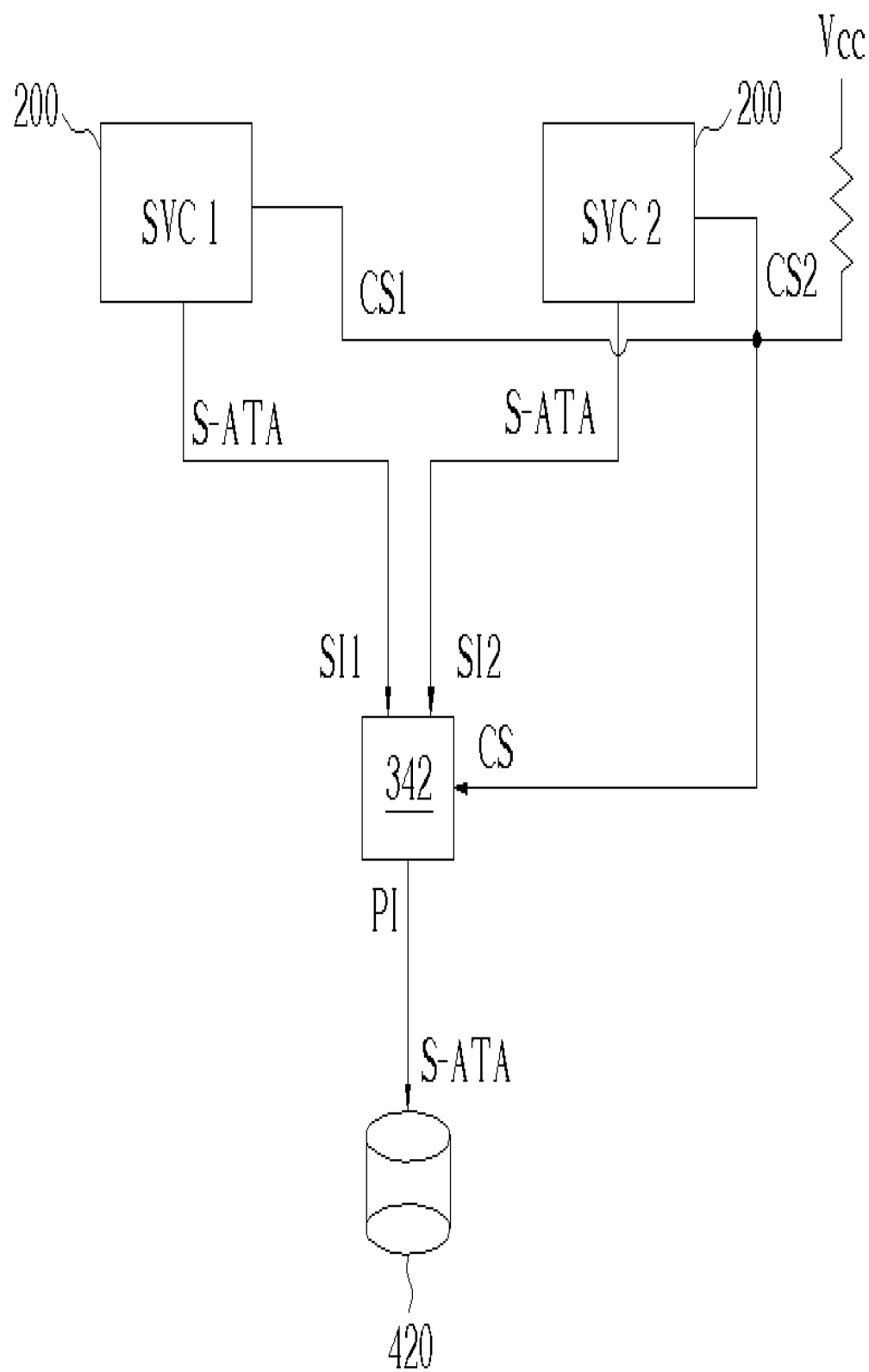


Fig. 4

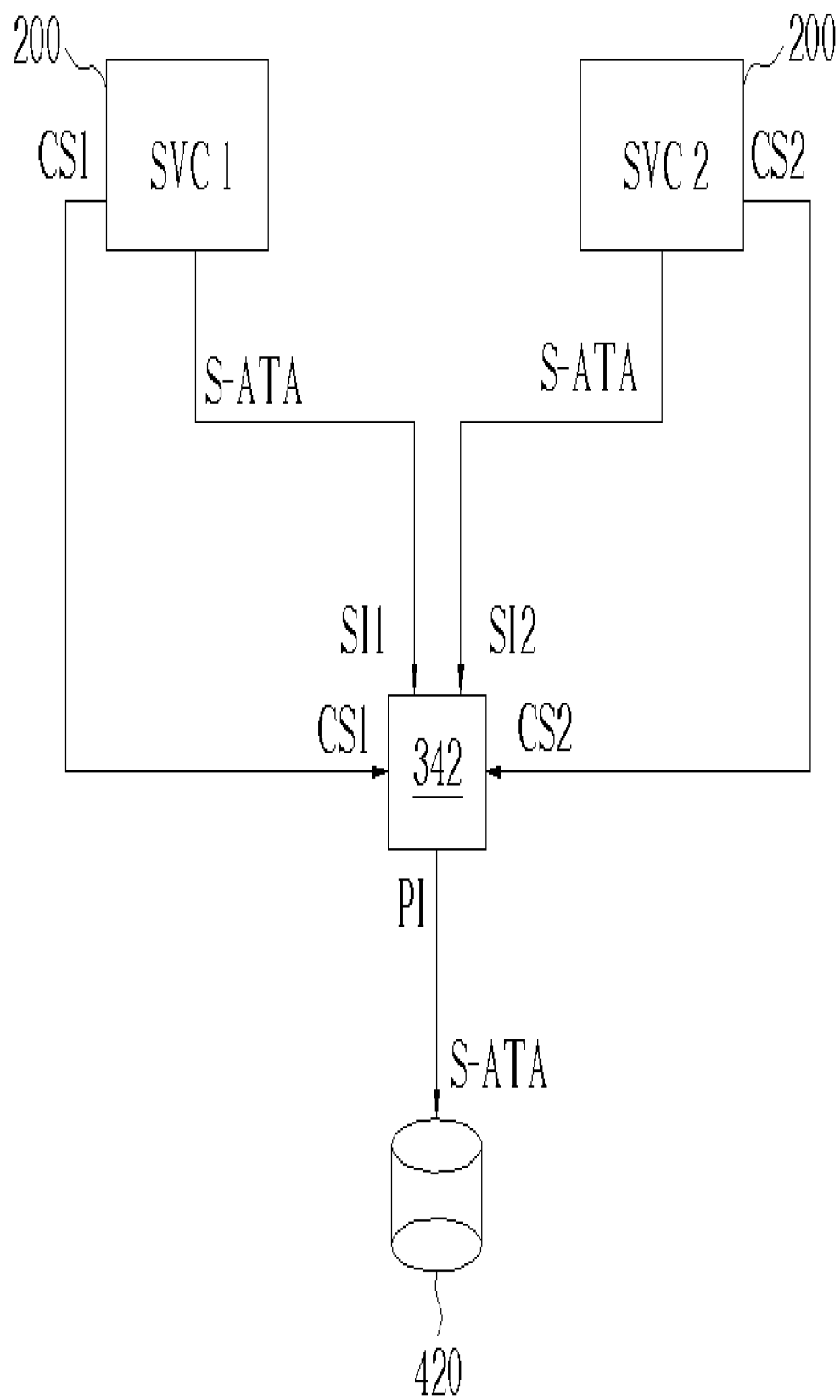


Fig. 5

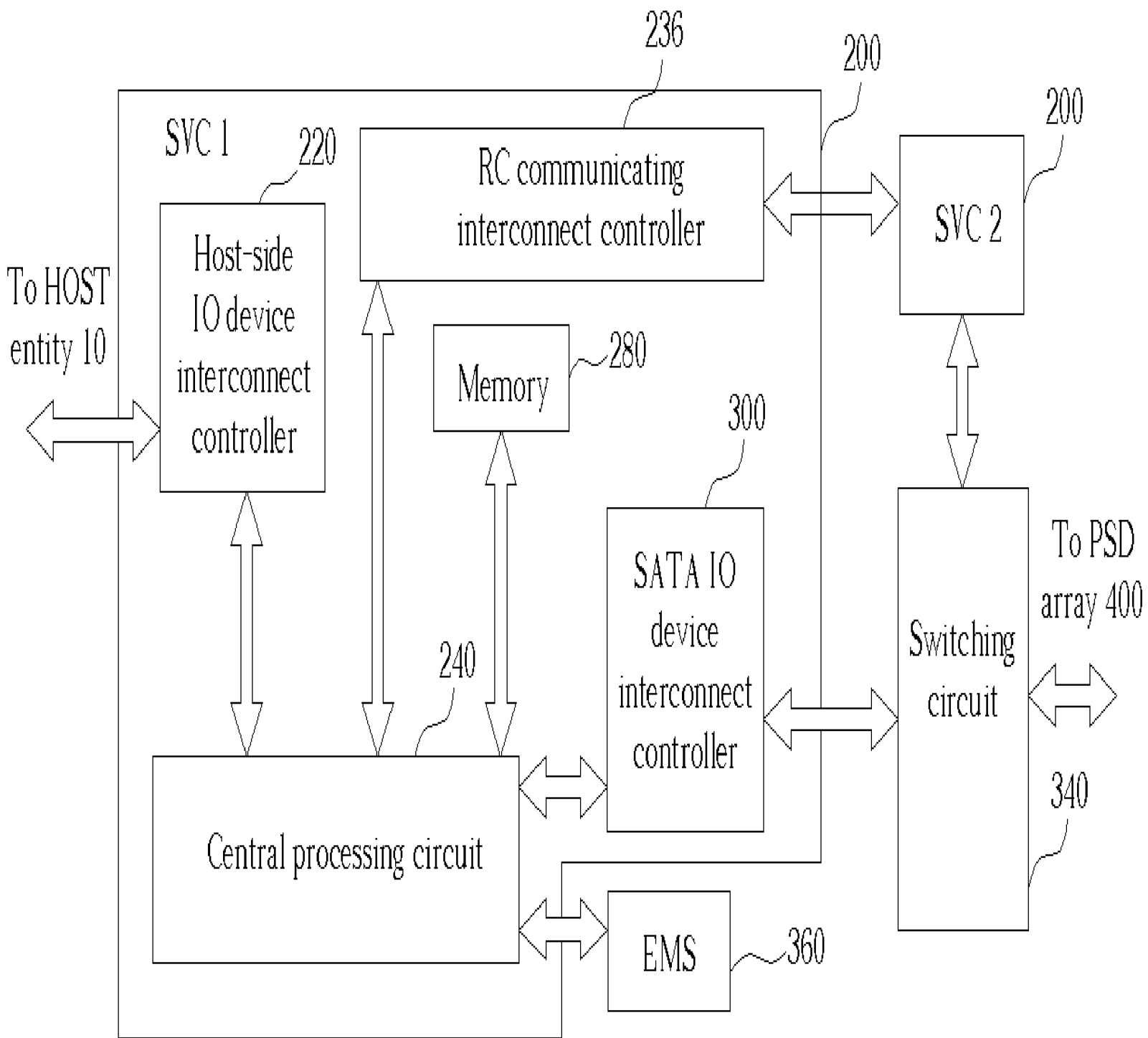


Fig. 6

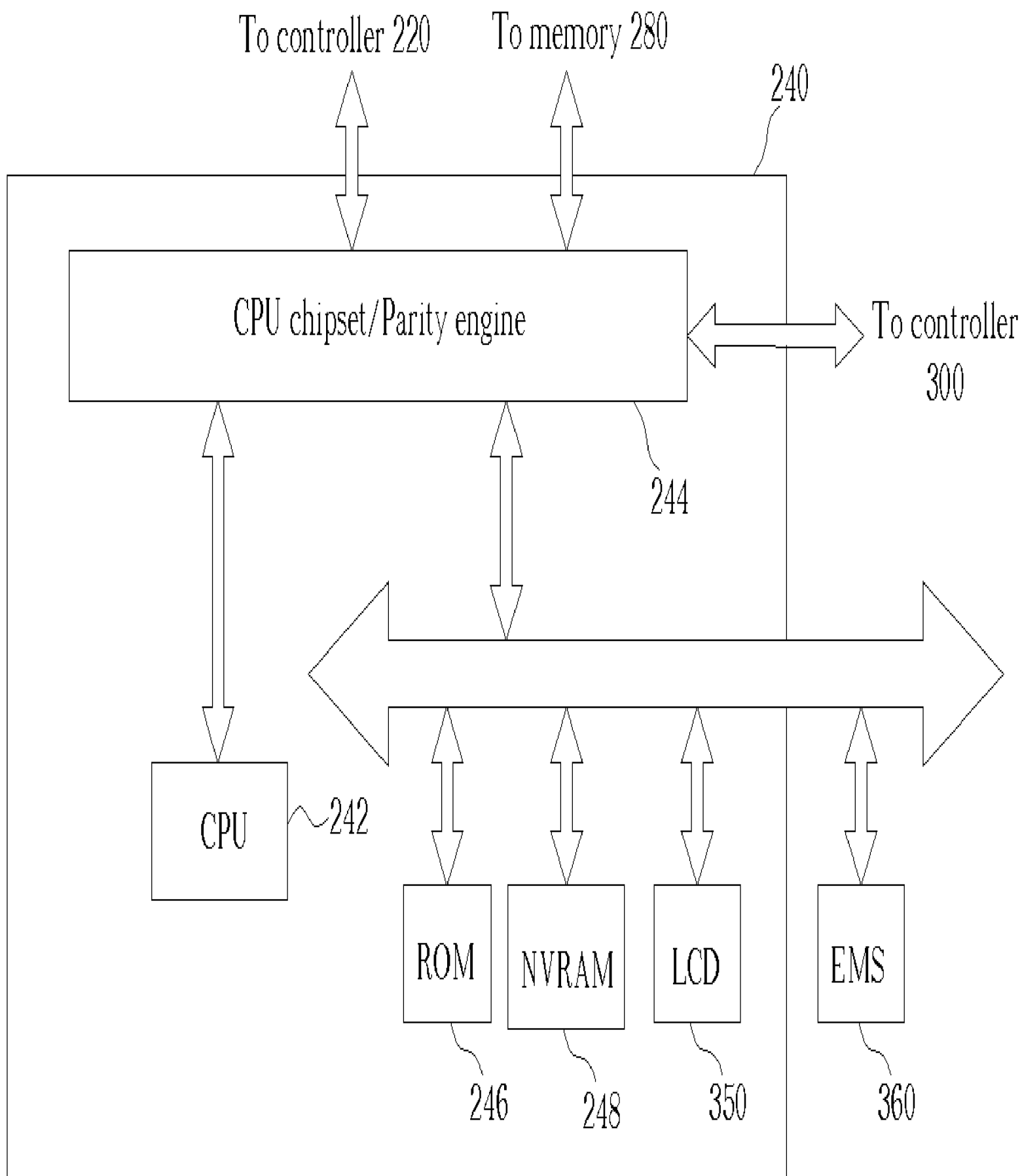


Fig. 7

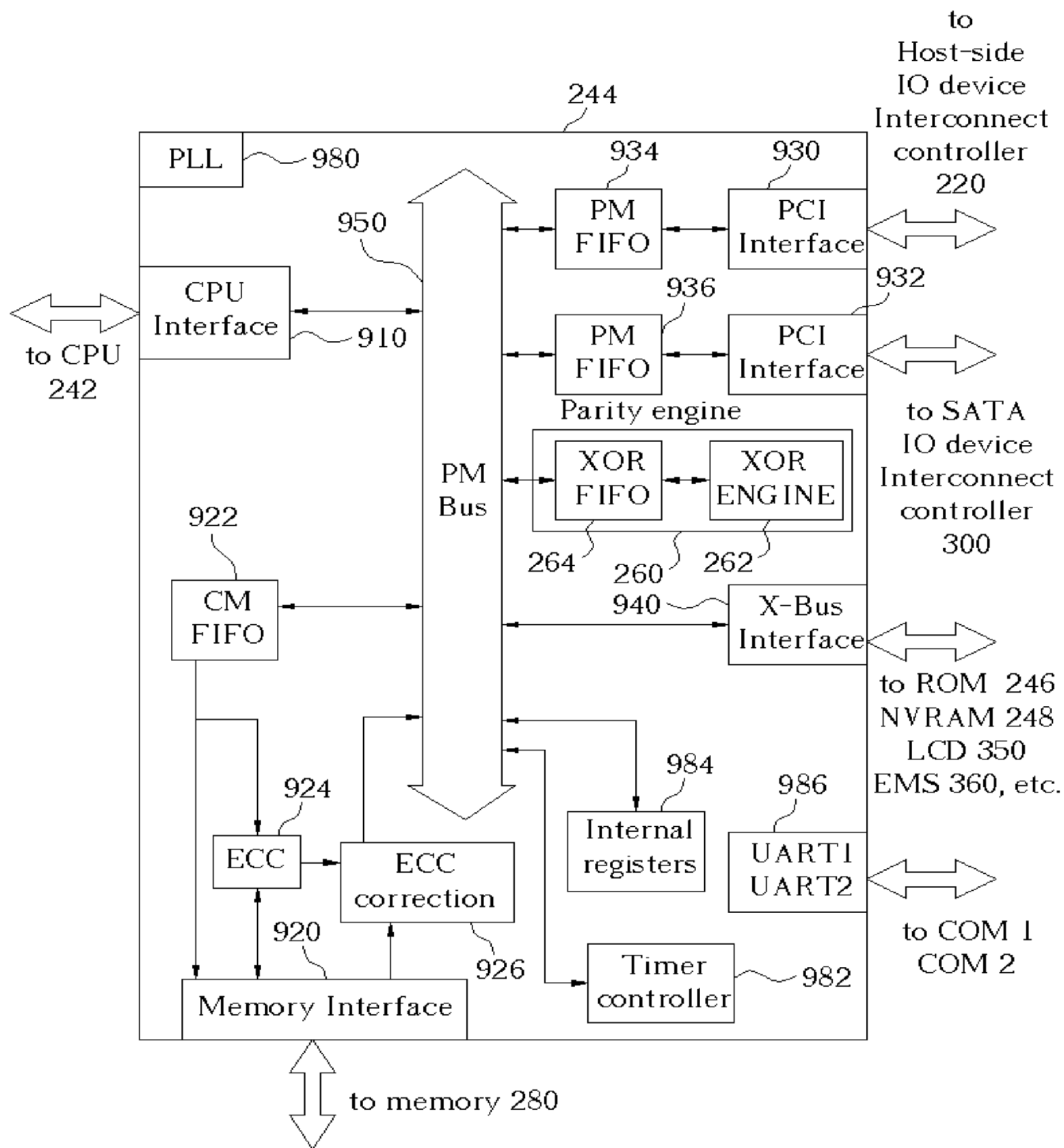


Fig. 8



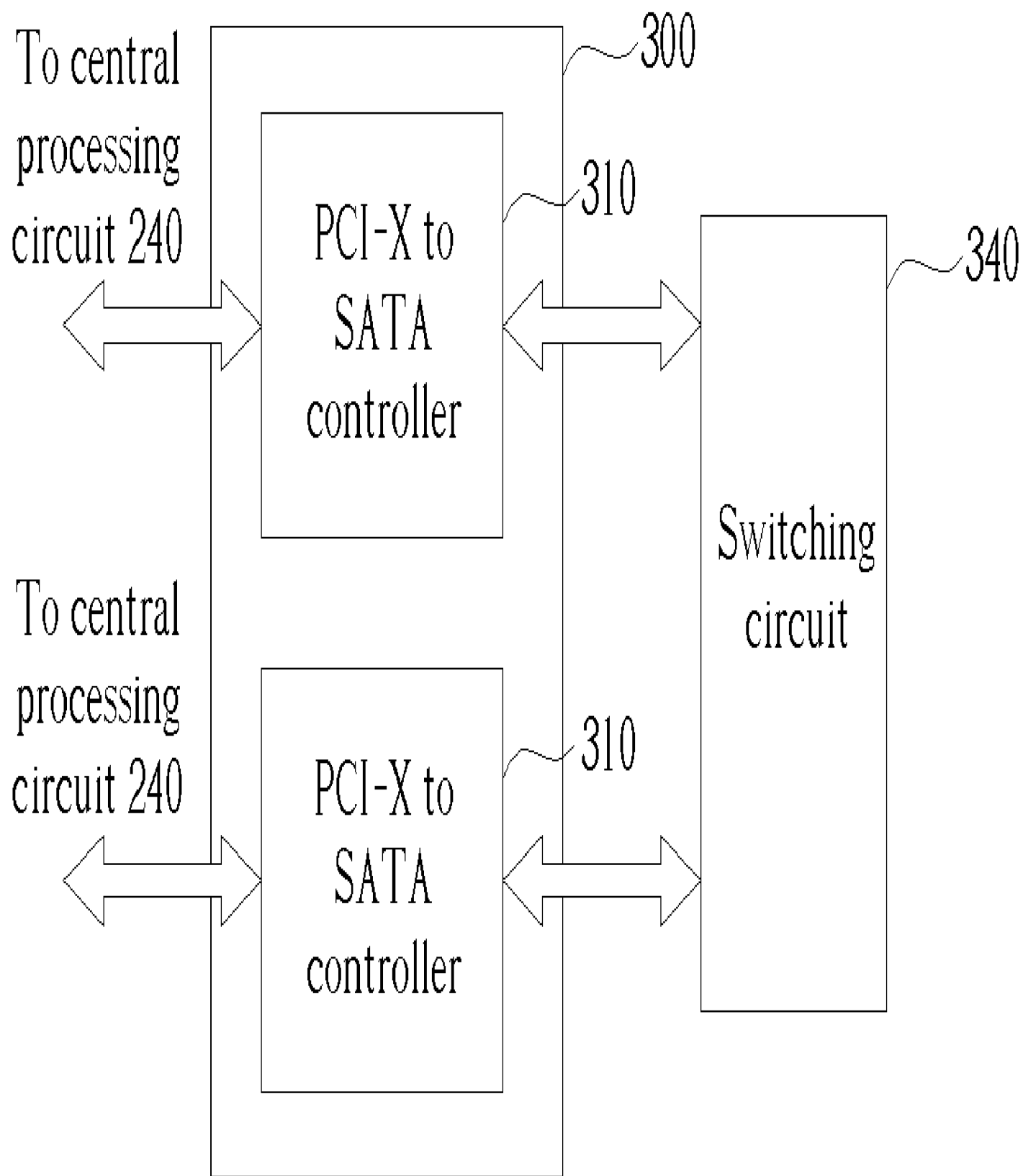


Fig. 9

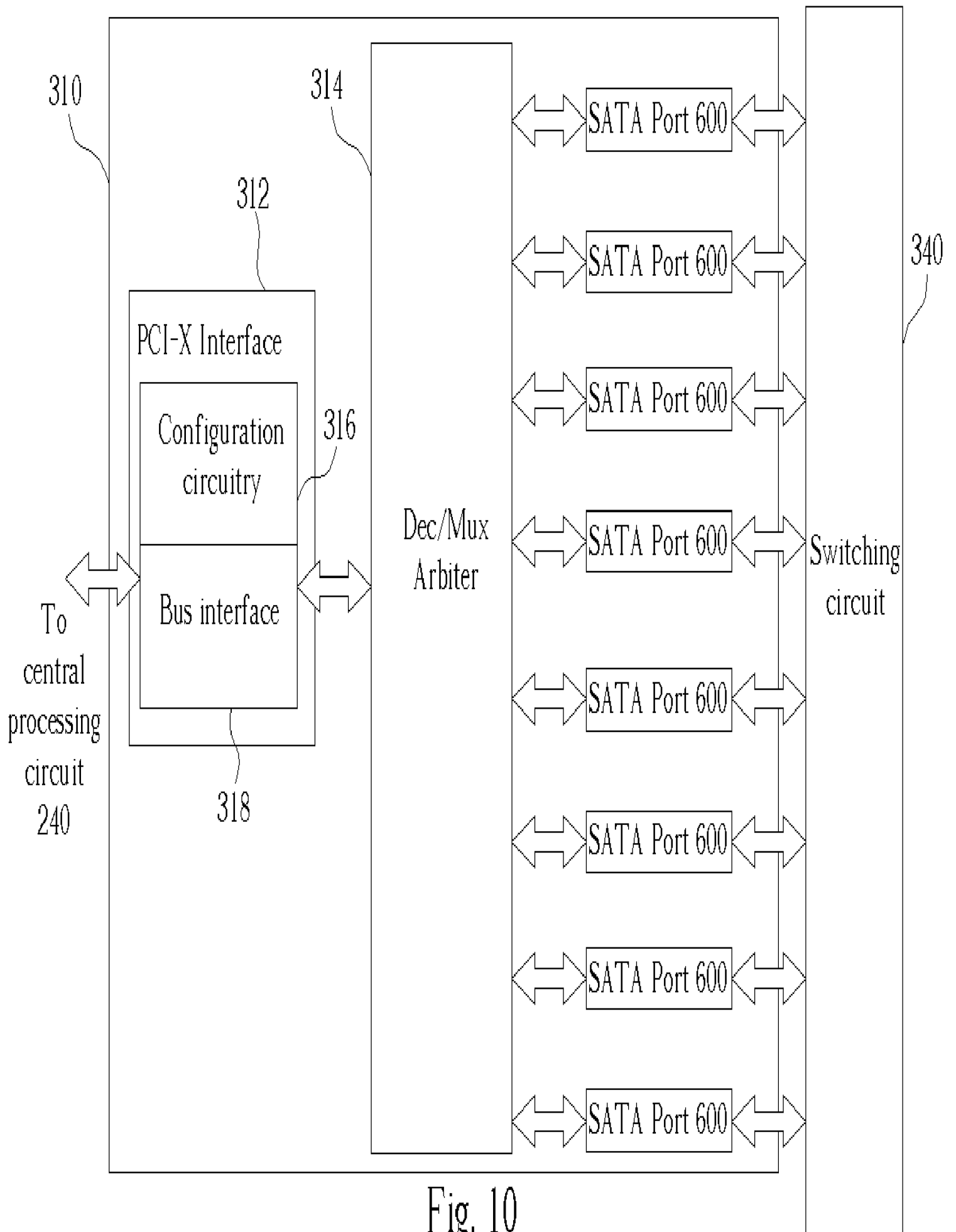


Fig. 10

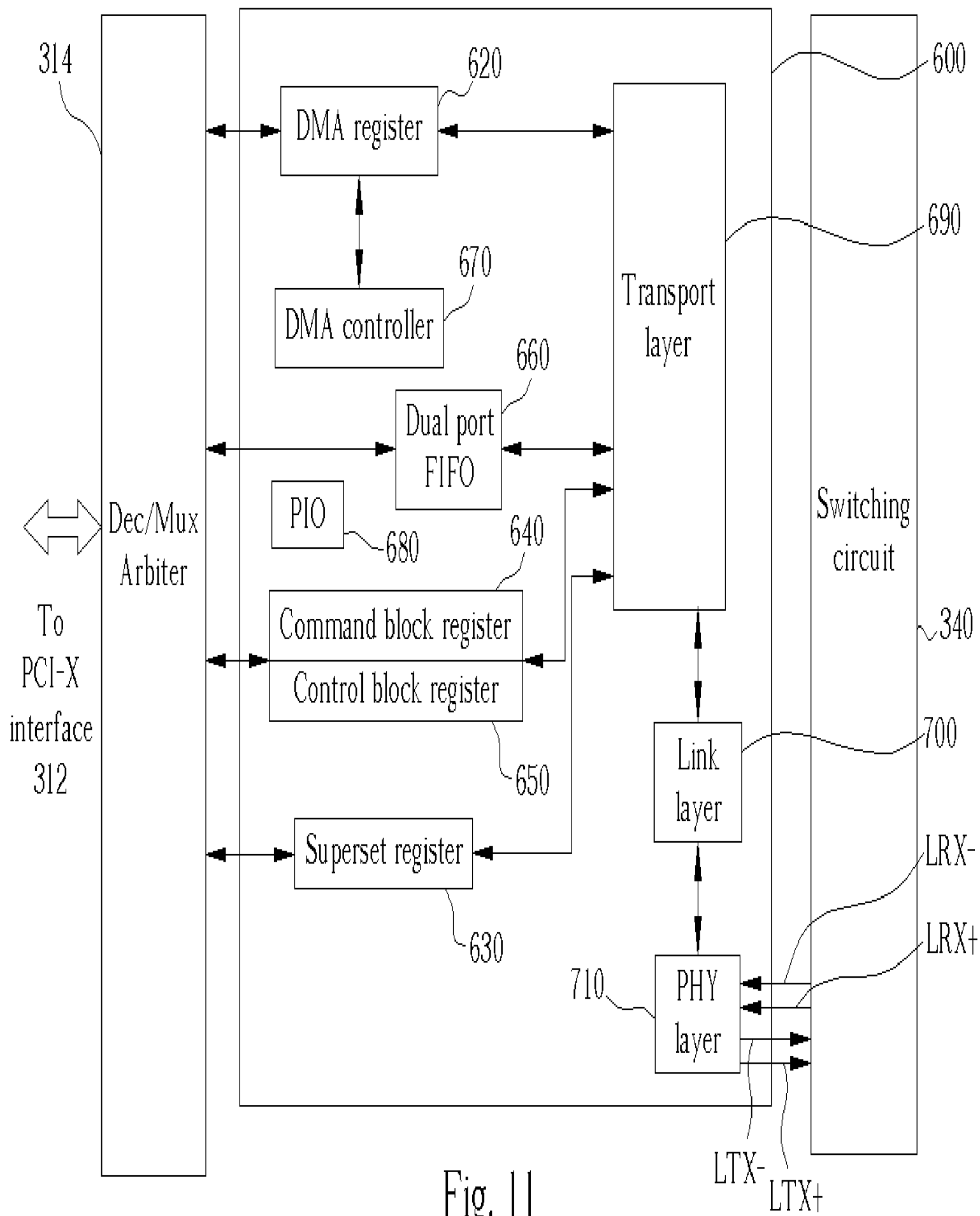


Fig. 11

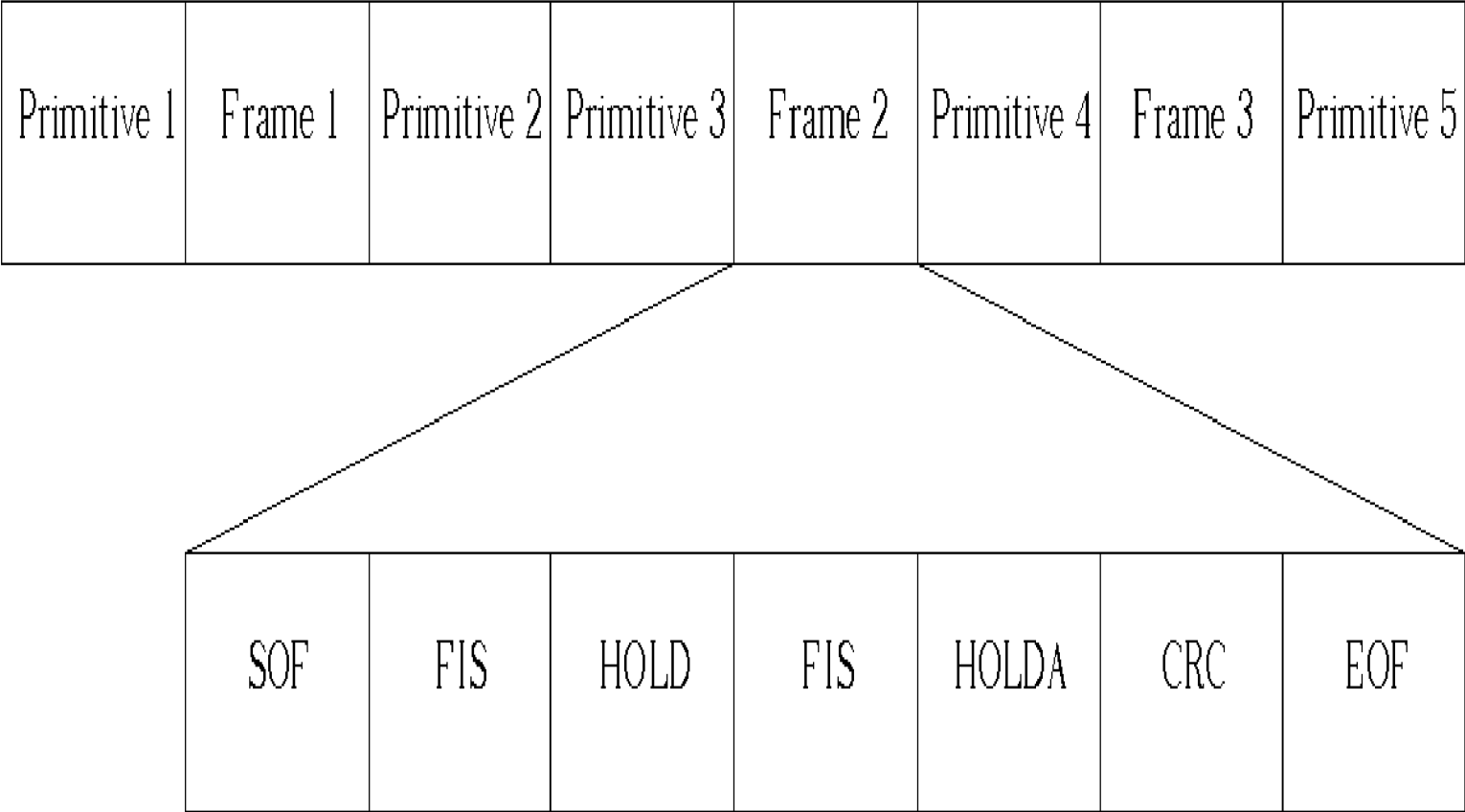


Fig. 12

0	Reserved (0)				Reserved (0)				R I D	Reserved (0)				FIS Type (41h)			
1	DMA buffer identifier Low																
2	DMA buffer identifier High																
3	Reserved (0)																
4	DMA buffer offset																
5	DMA transfer count																
6	Reserved (0)																

Fig. 13

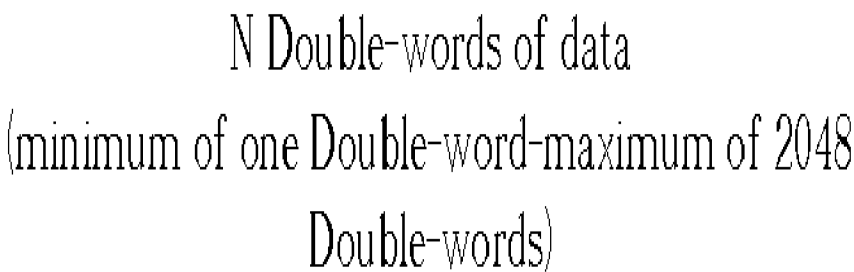


Fig. 14

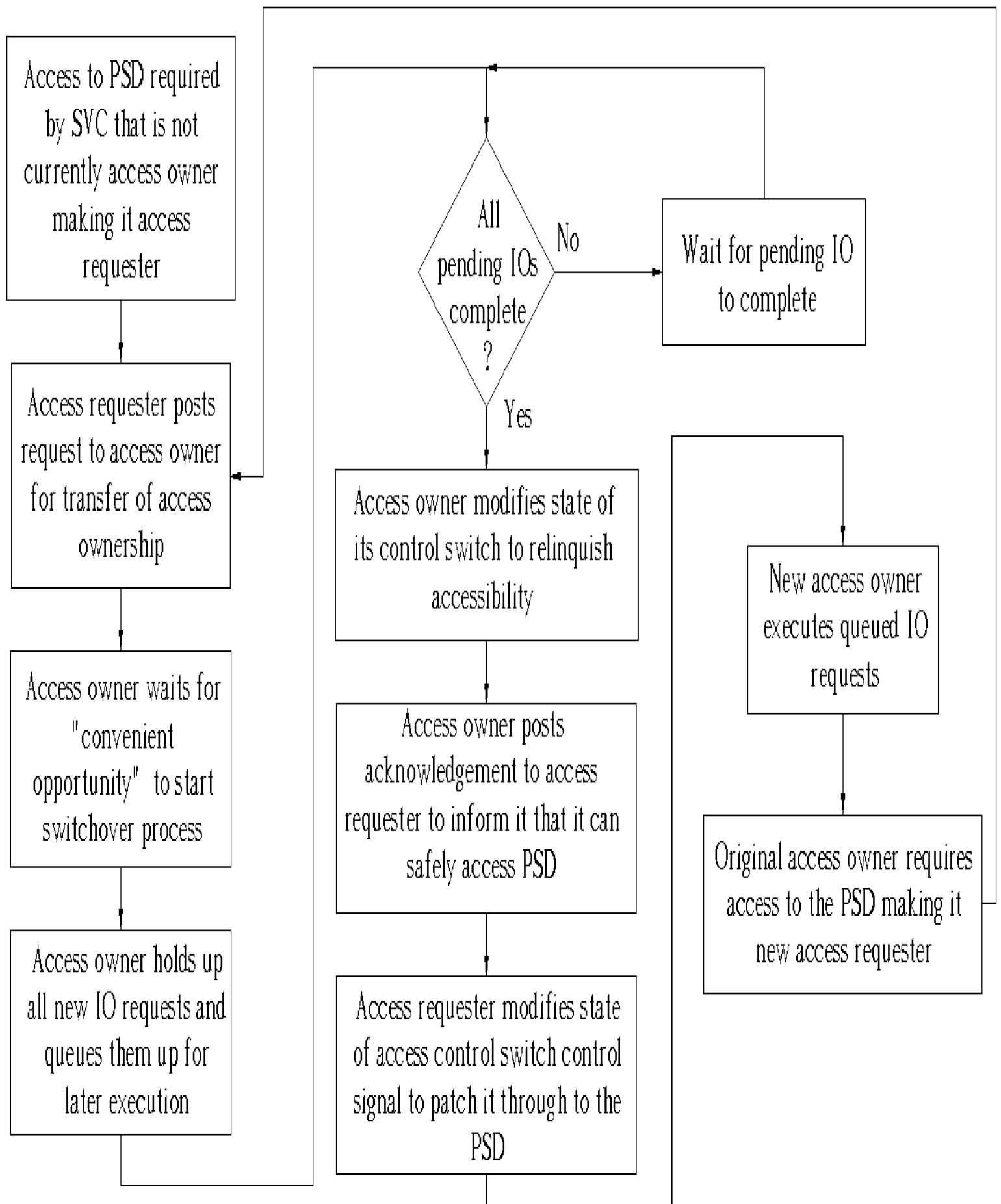


Fig. 15

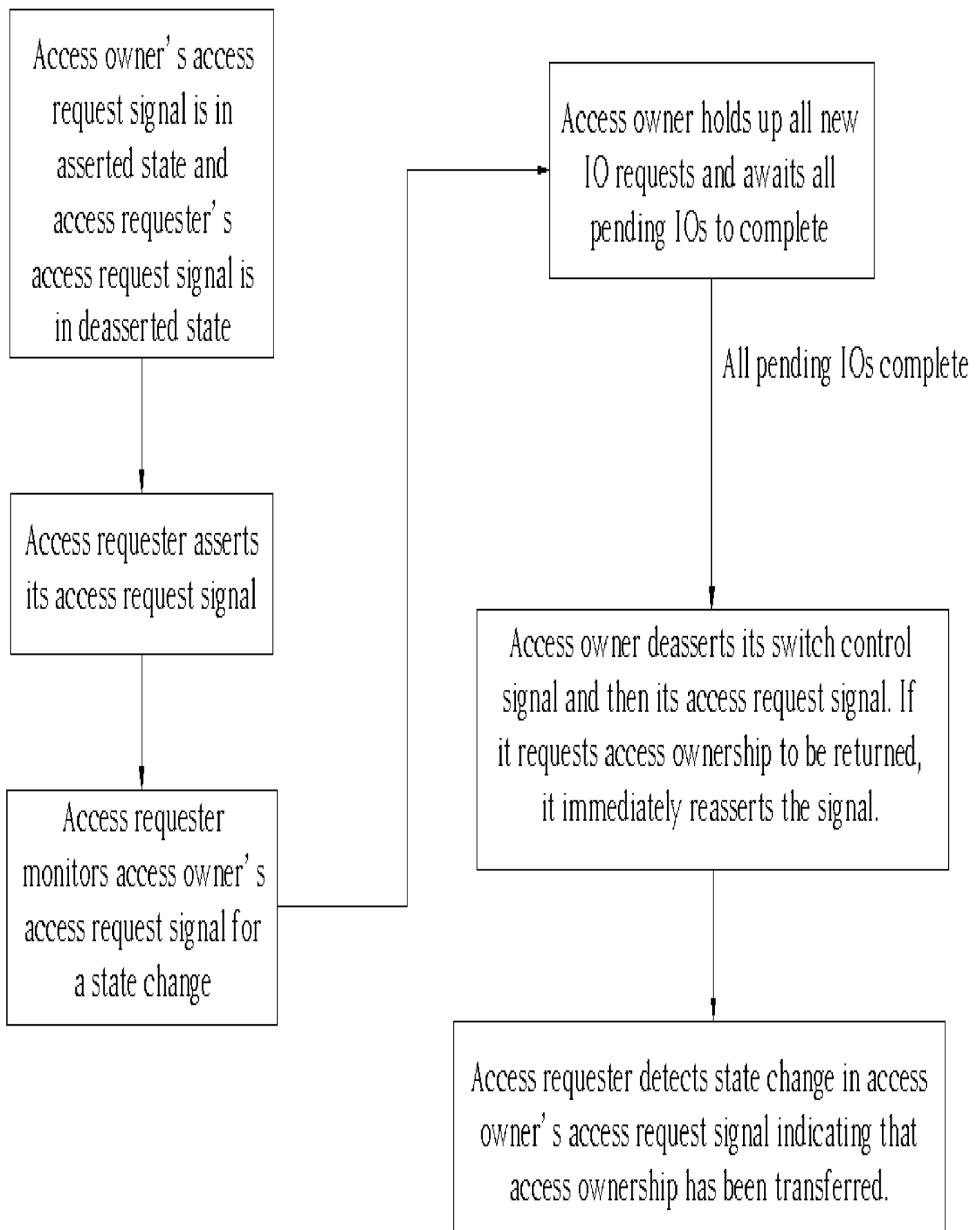
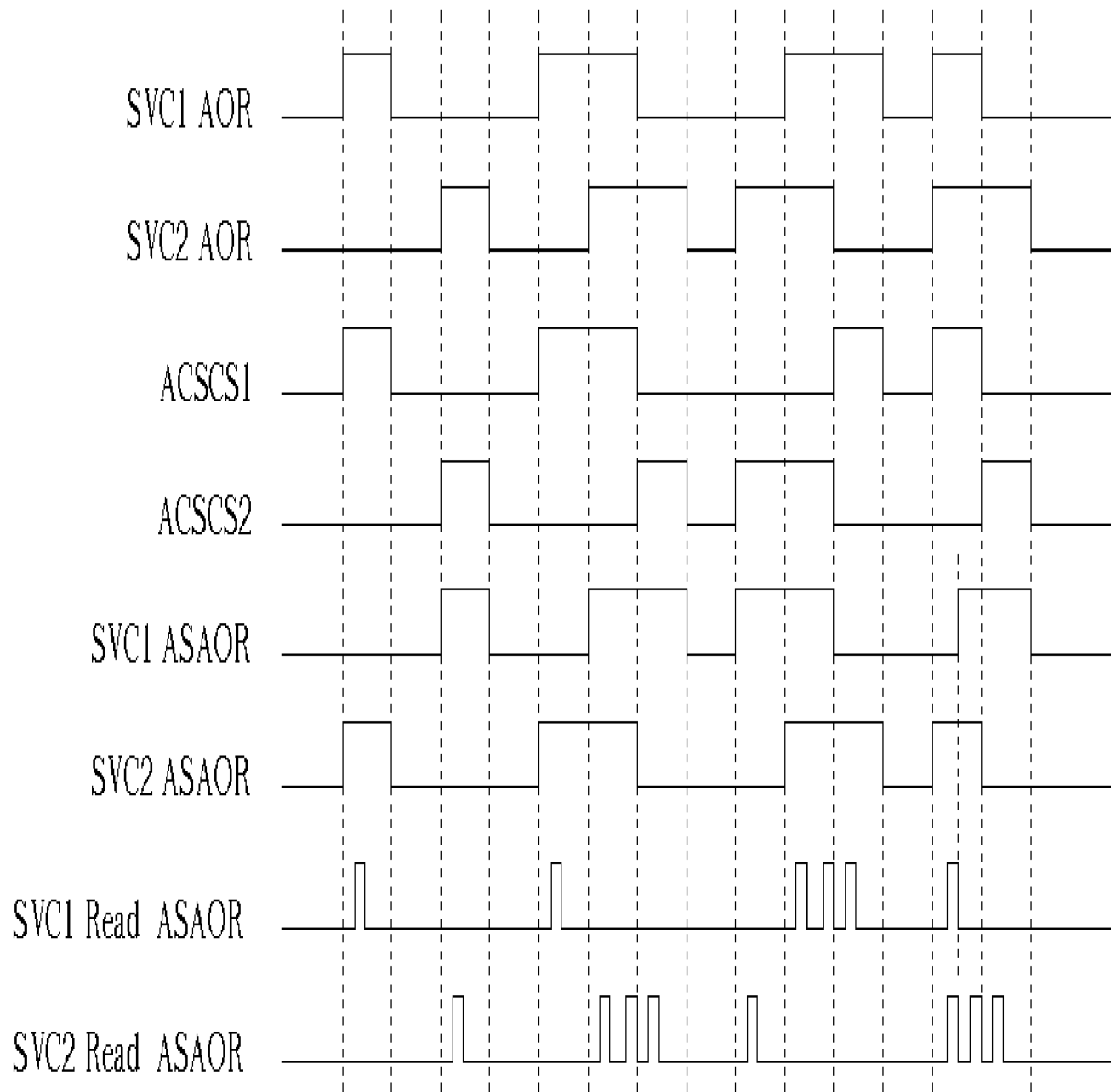


Fig. 16





SVC1 AOR ; SVC1' s AOR Signal

ACSCS1 ; SVC1' s Access Control  
Switch Control Signal

SVC1 ASAOR ; SVC1' s Alternate SVC AOR  
Signal

SVC1 Read ASAOR ; SVC1 Read ASAOR State  
Pulse

SVC2 AOR ; SVC2' s AOR Signal

ACSCS2 ; SVC2' s Access Control  
Switch Control Signal

SVC2 ASAOR ; SVC2' s Alternate SVC  
AOR Signal

SVC2 Read ASAOR ; SVC2 Read ASAOR State  
Pulse

Fig. 17

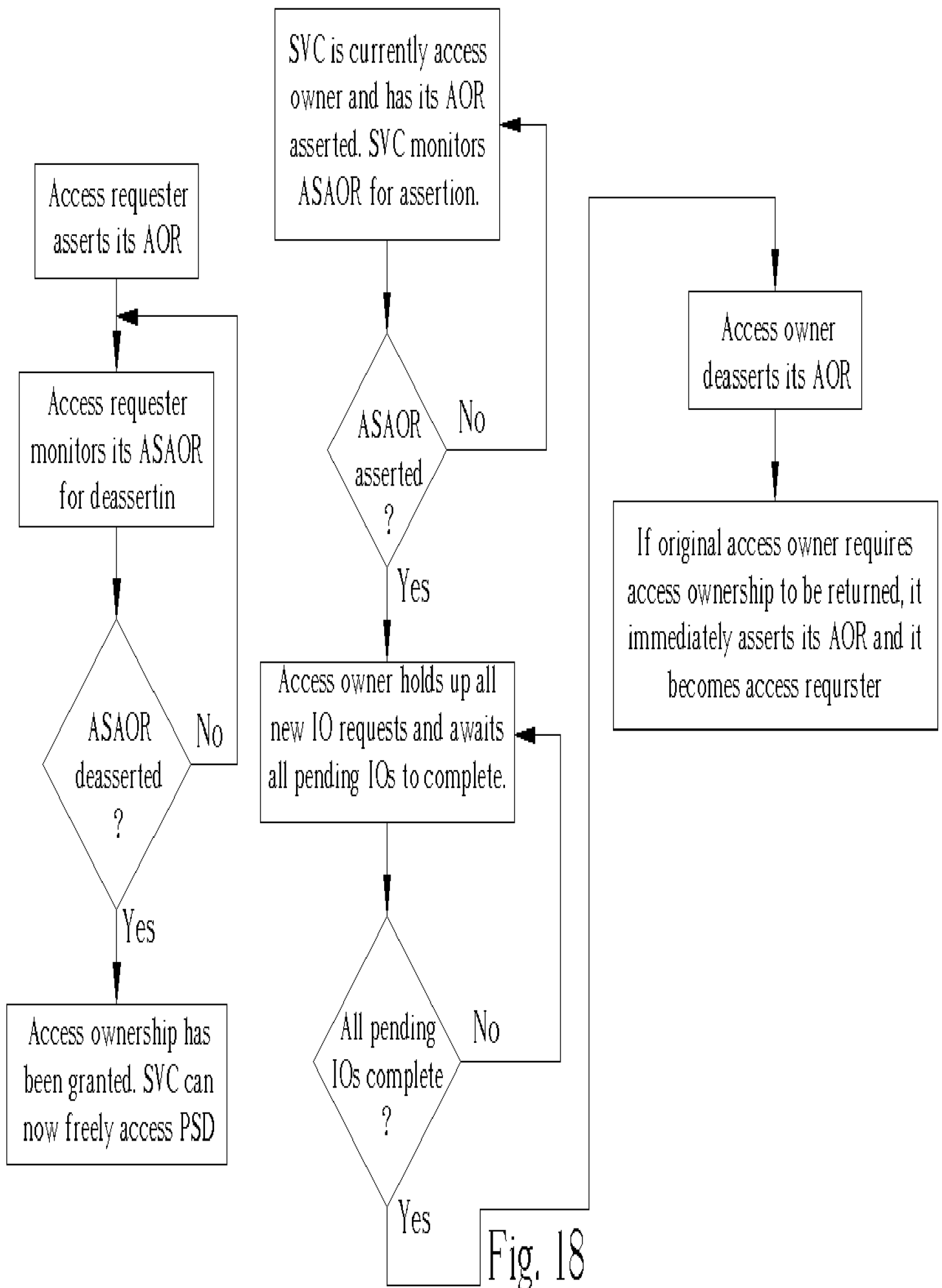


Fig. 18

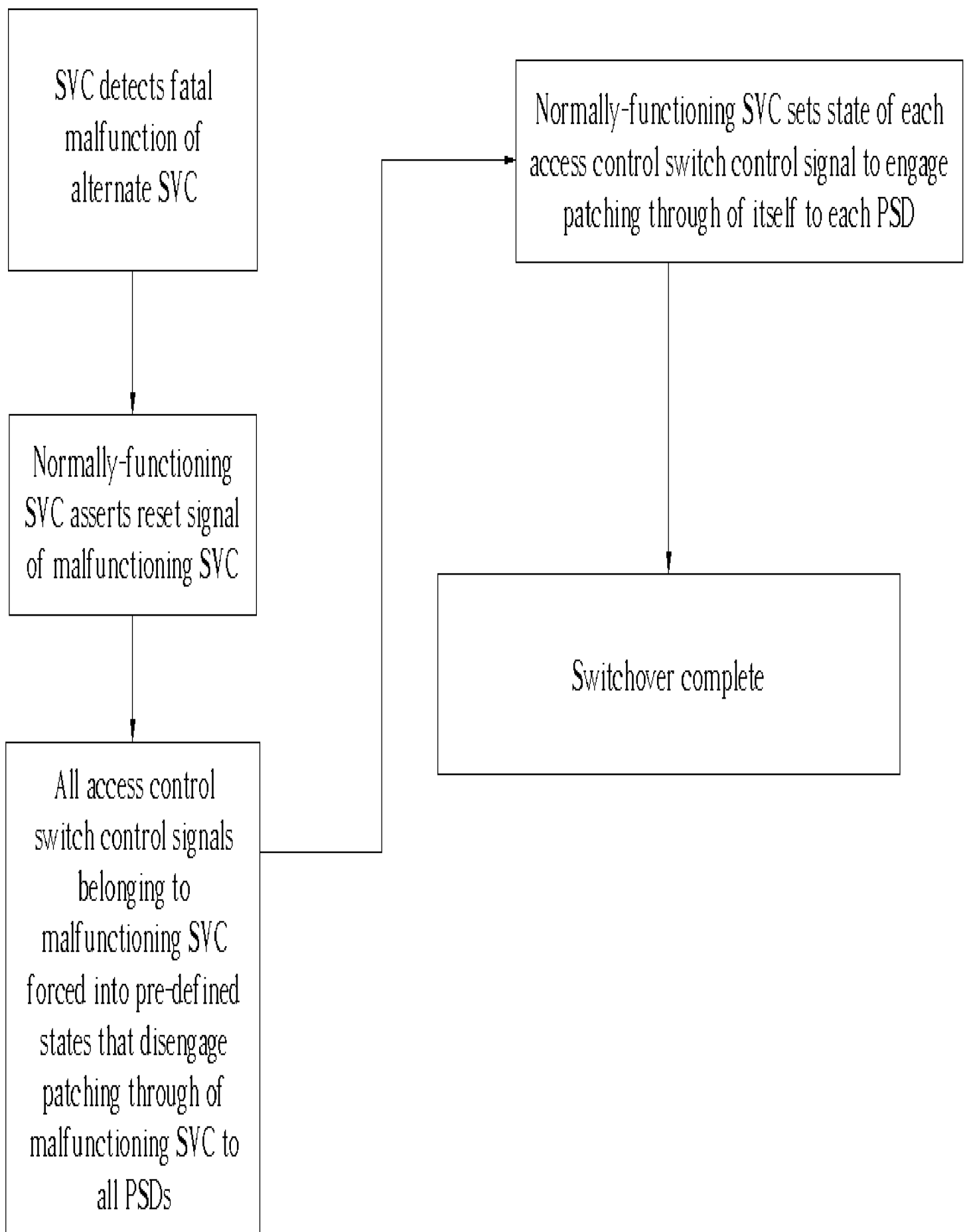


Fig. 19

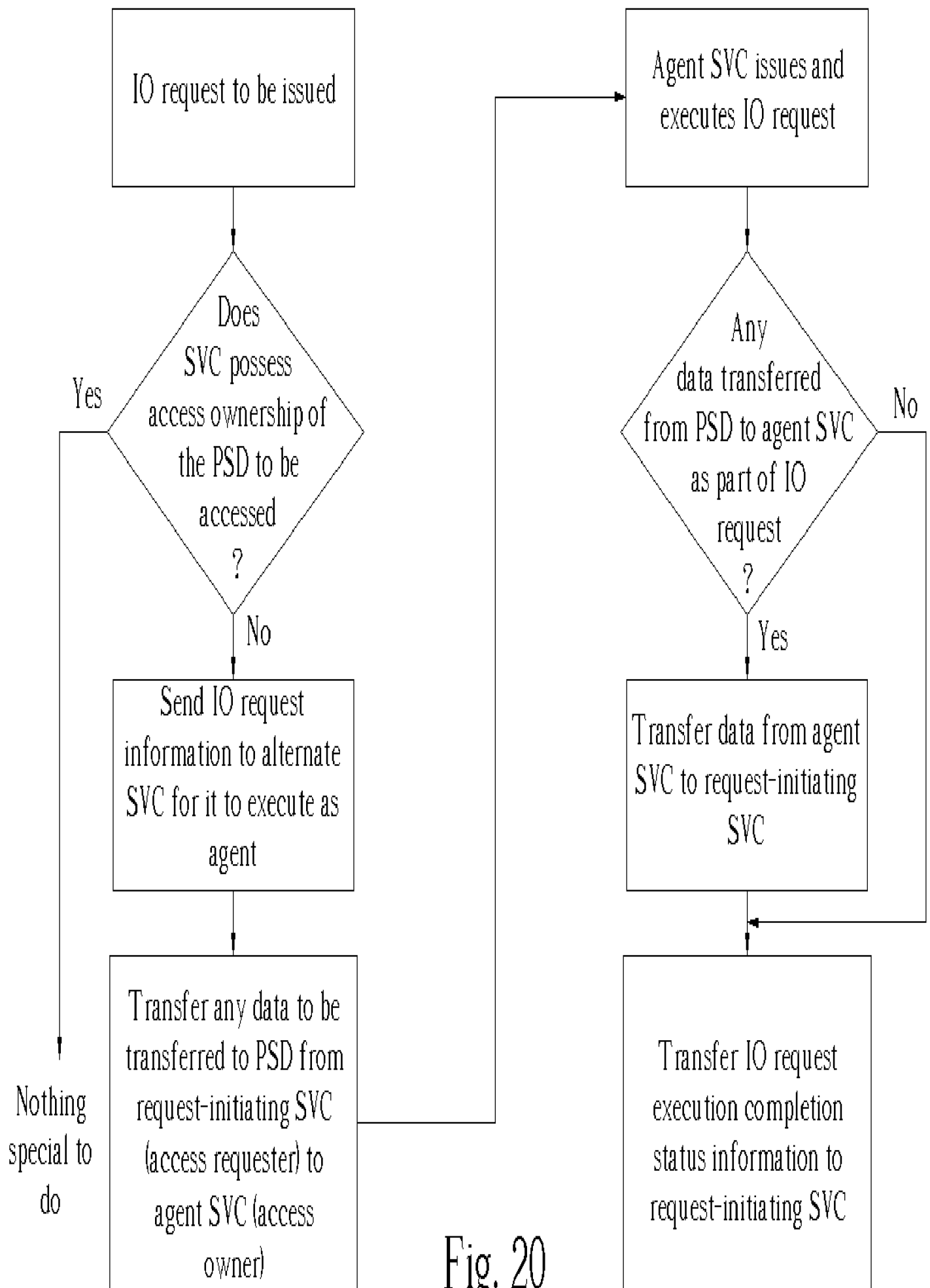


Fig. 20

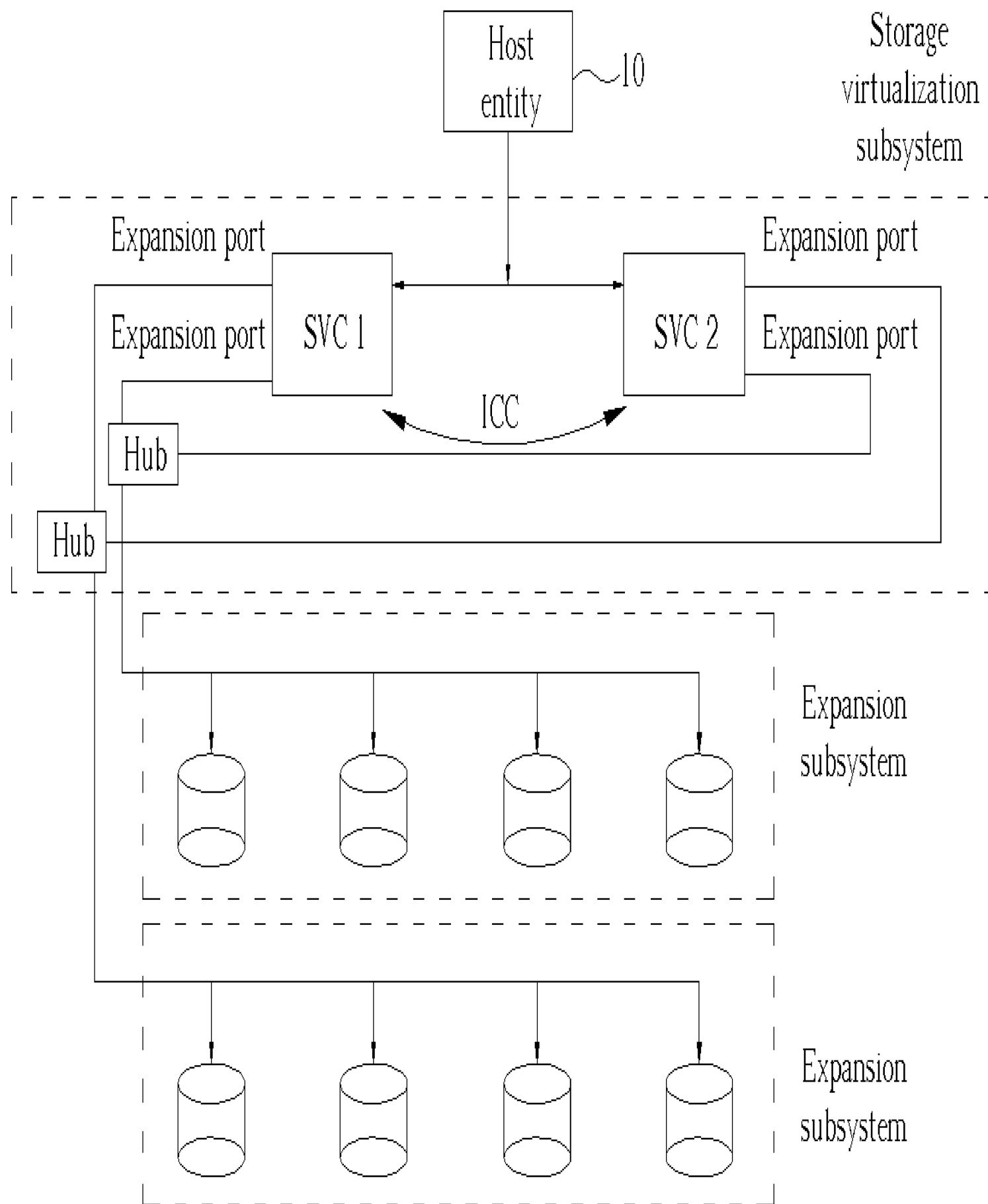


Fig. 21

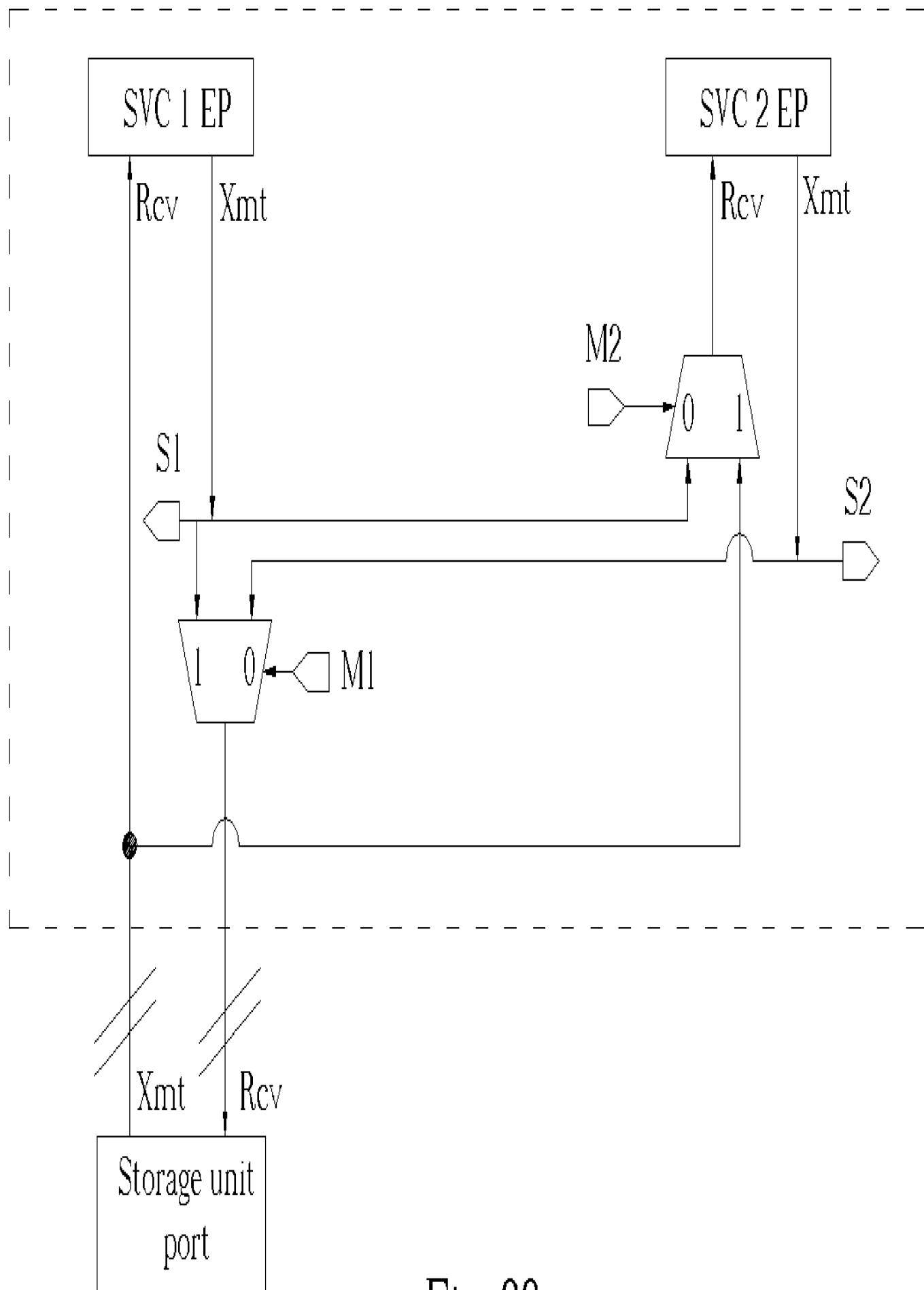


Fig. 22

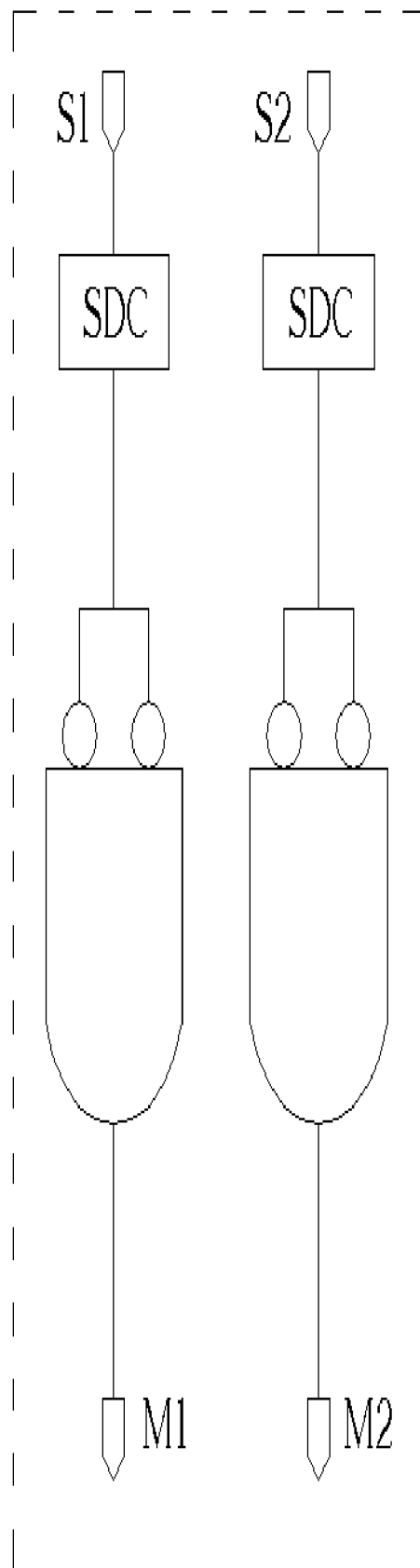


Fig. 23

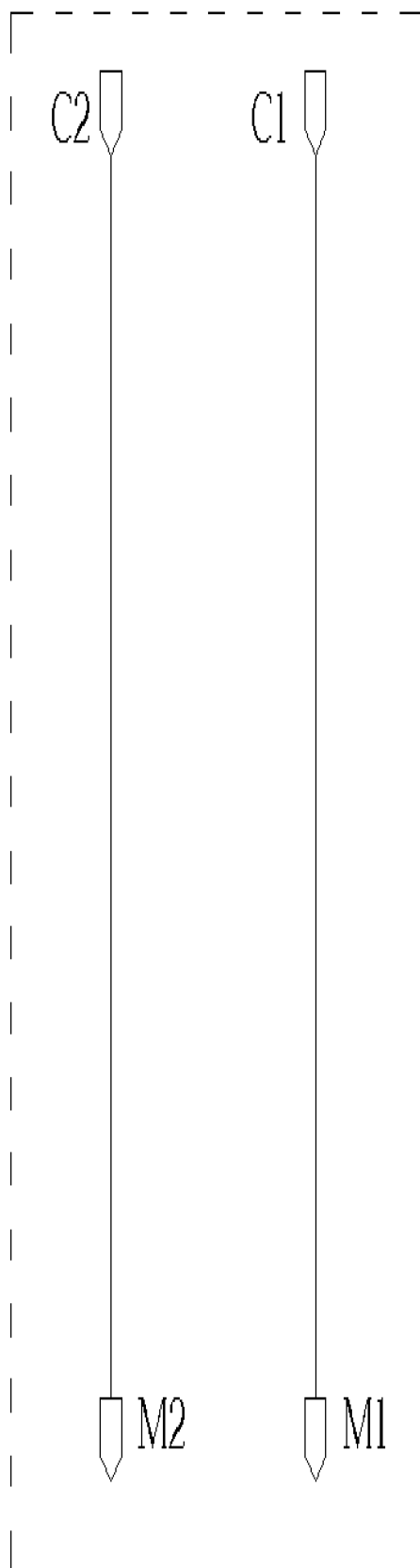


Fig. 24



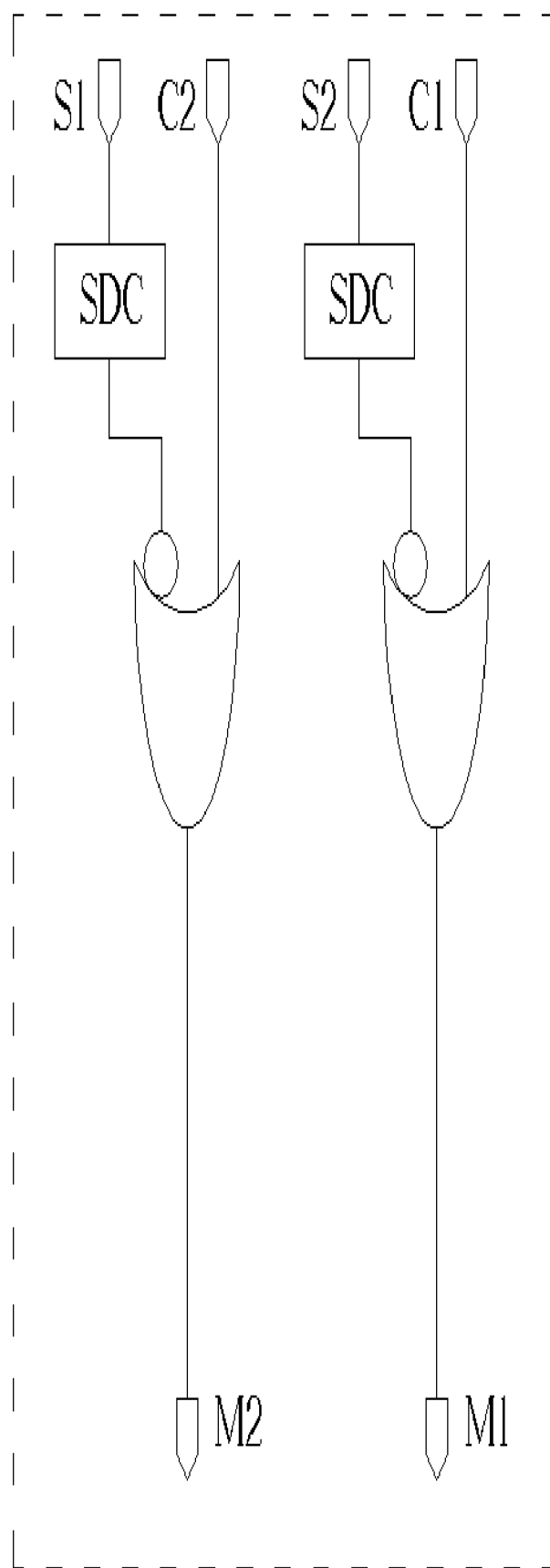


Fig. 25

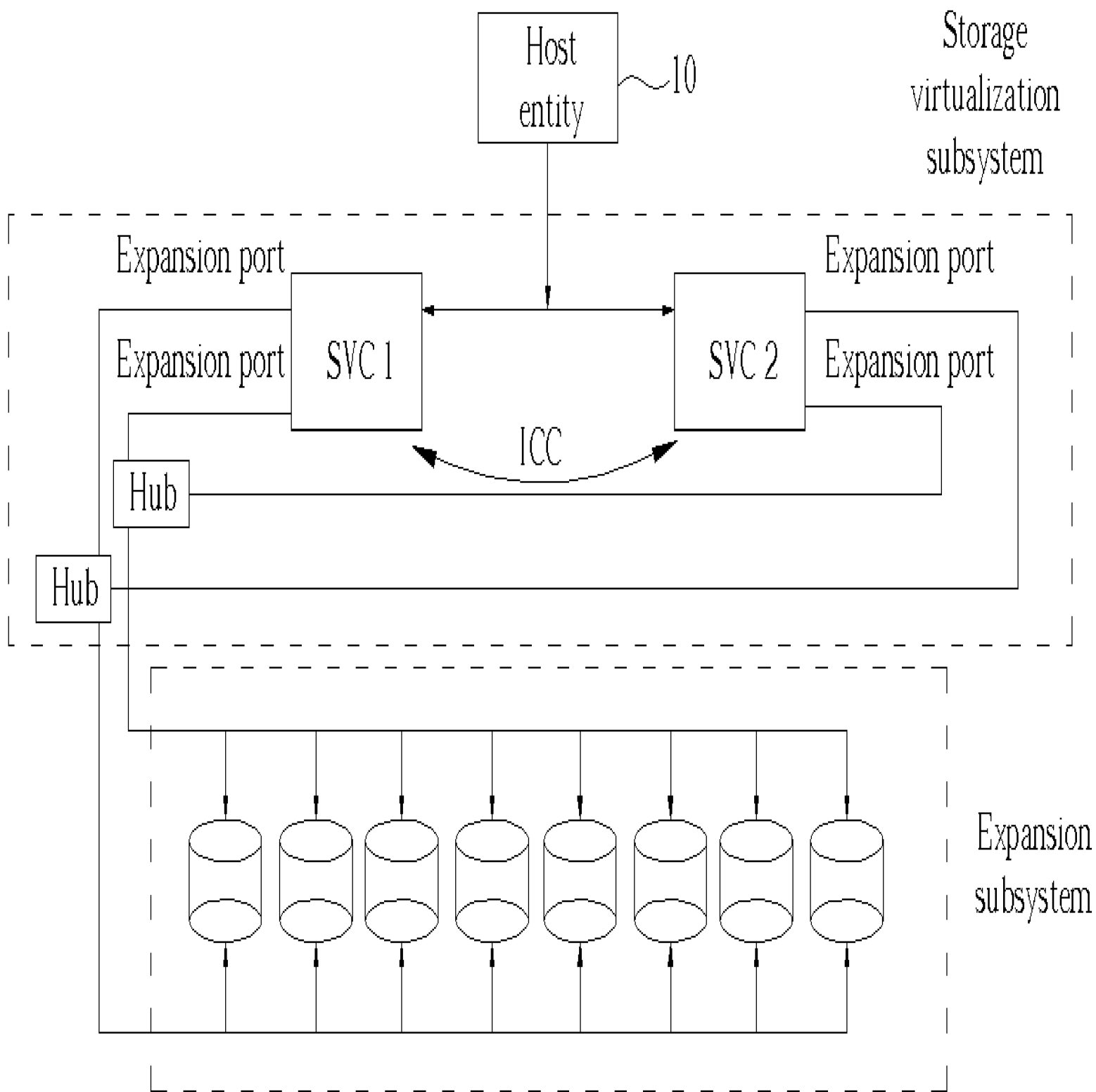


Fig. 26

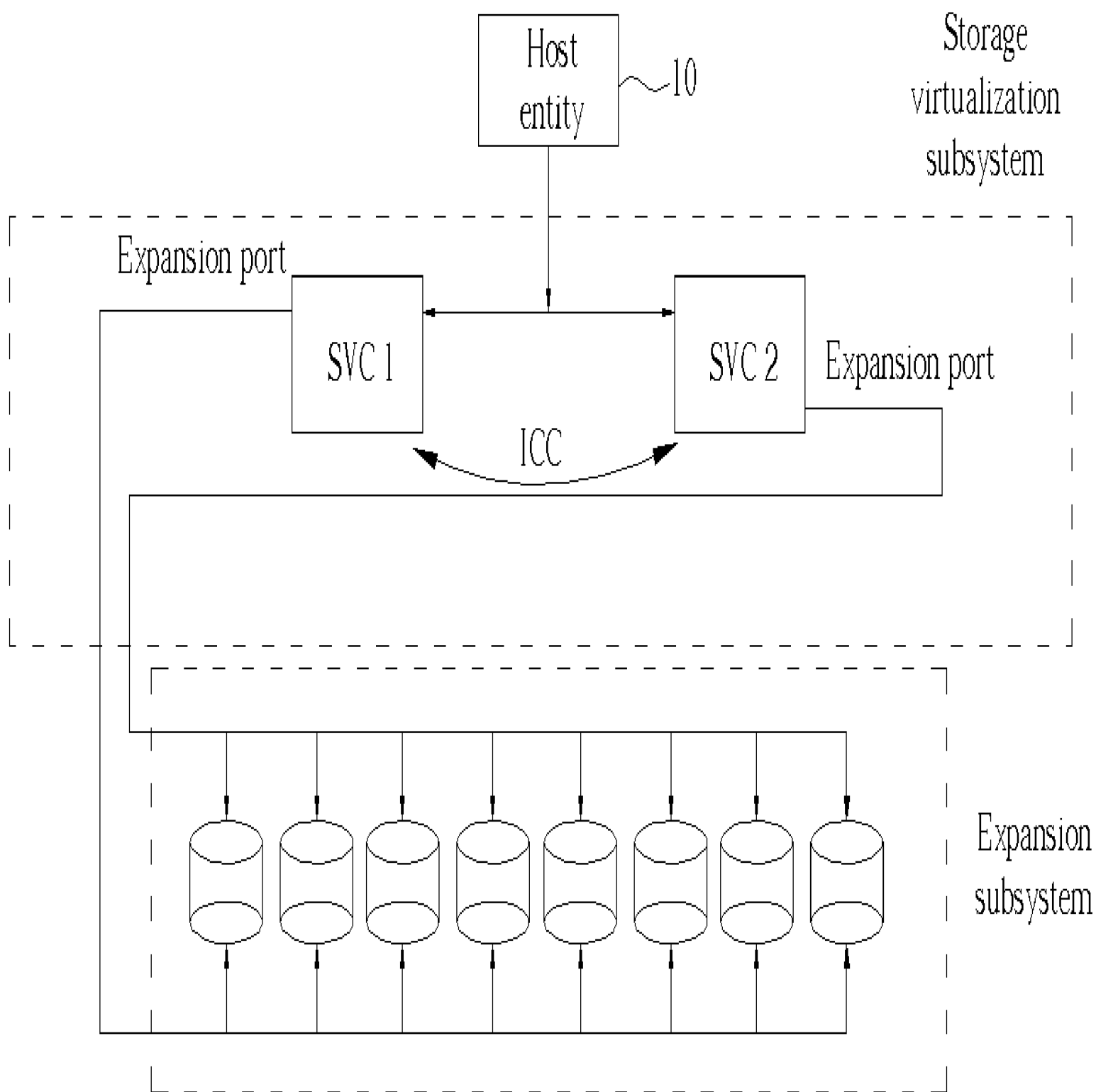


Fig. 27

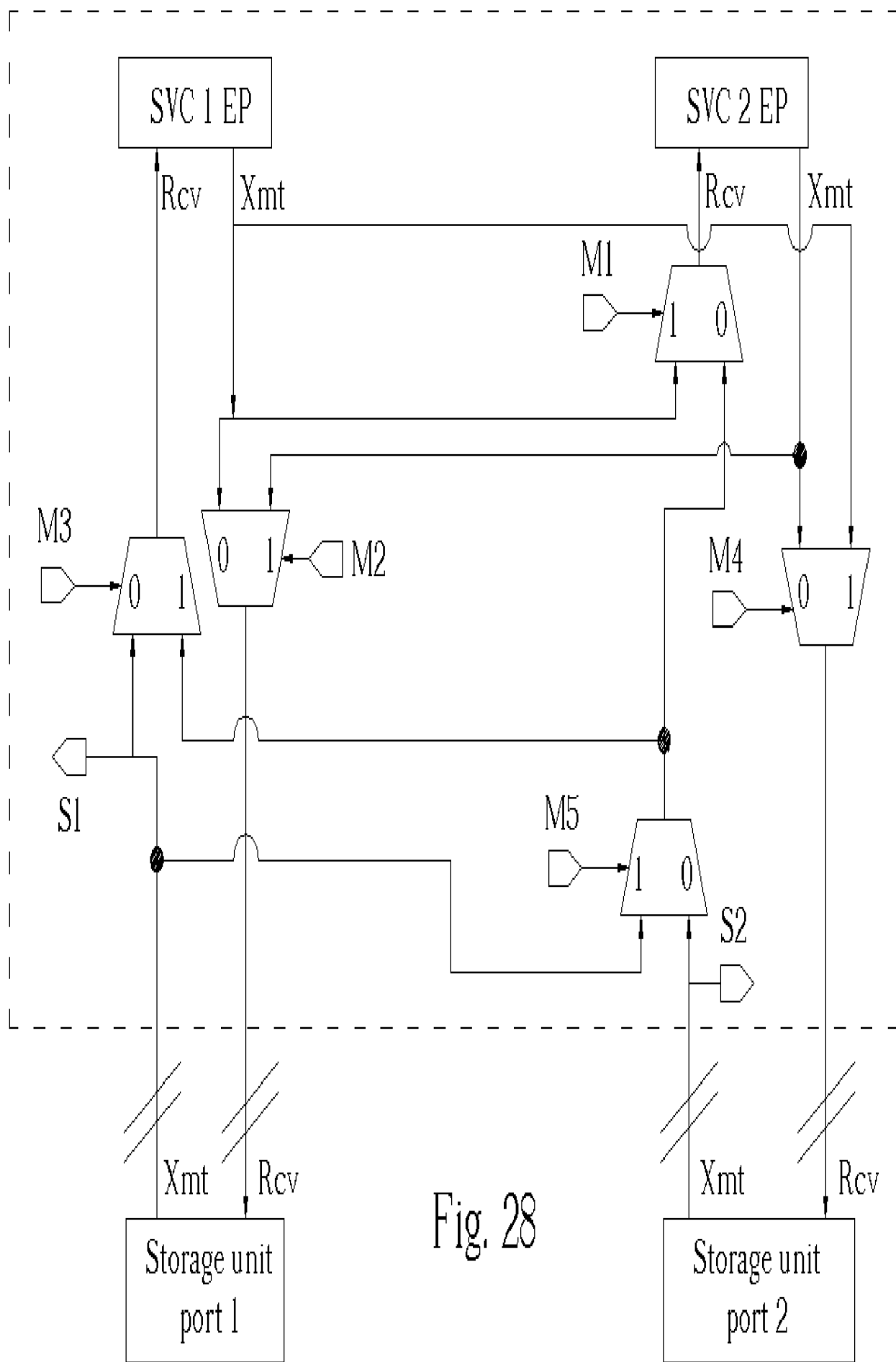


Fig. 28

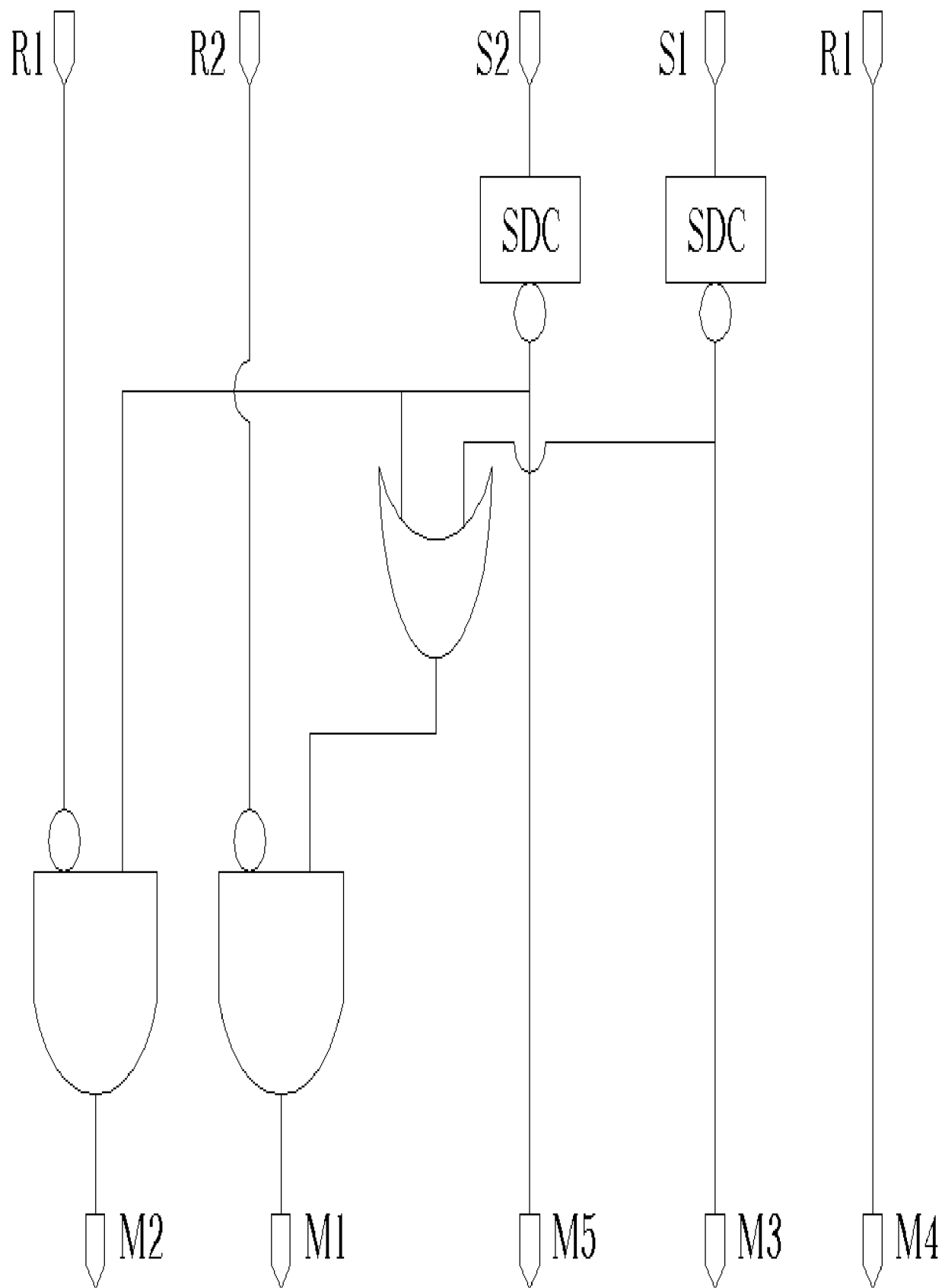


Fig. 29

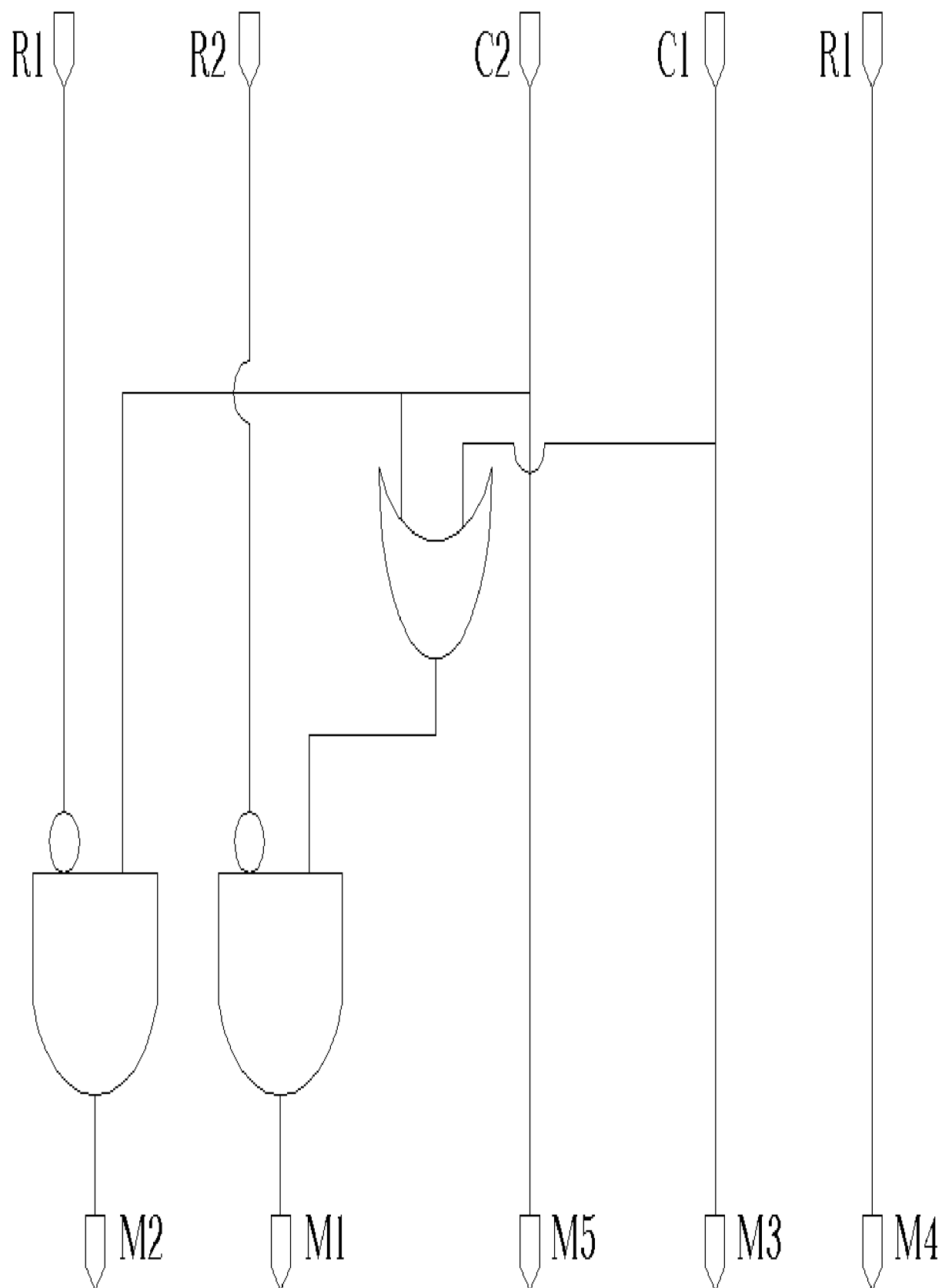


Fig. 30

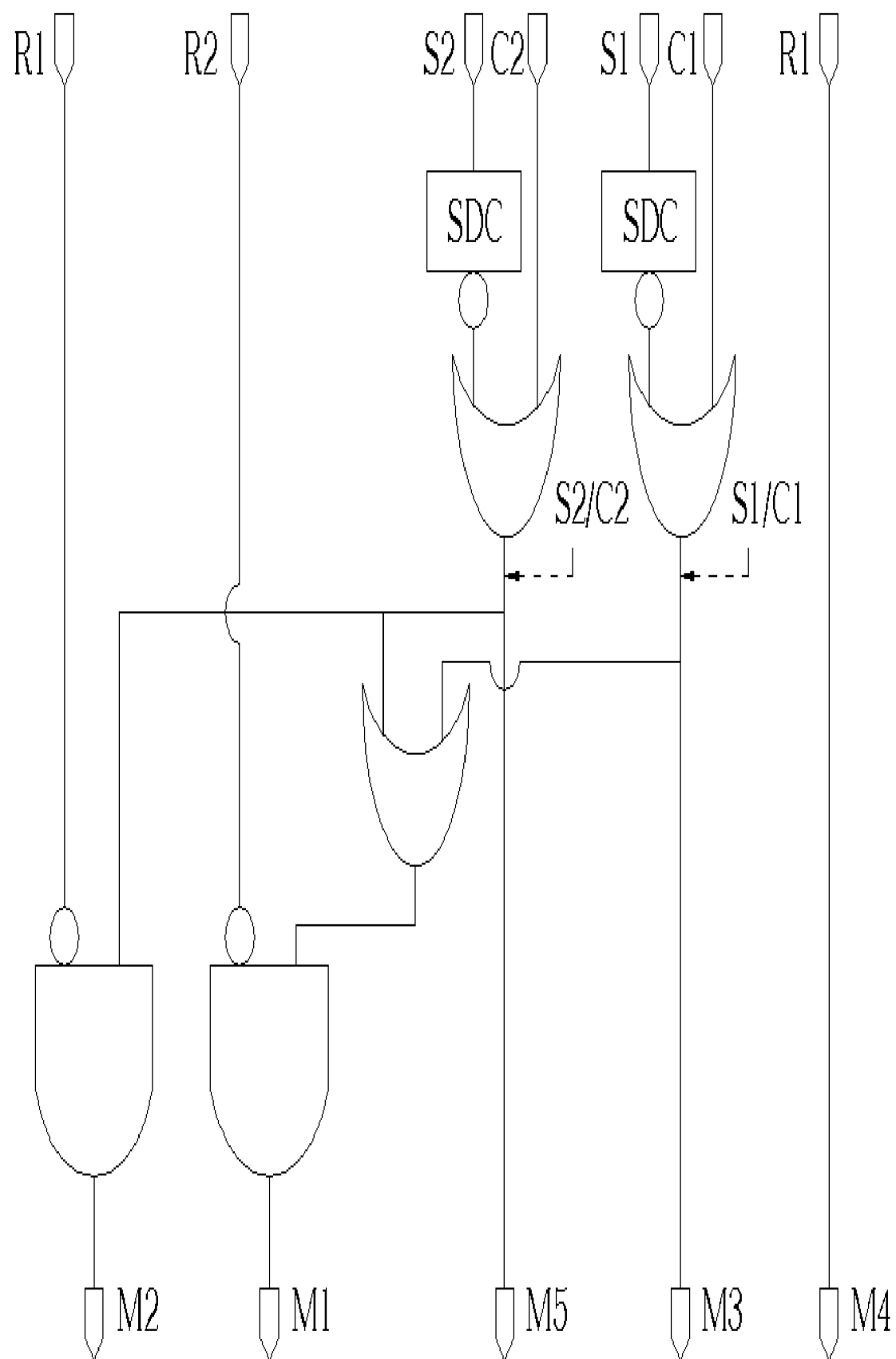


Fig. 31

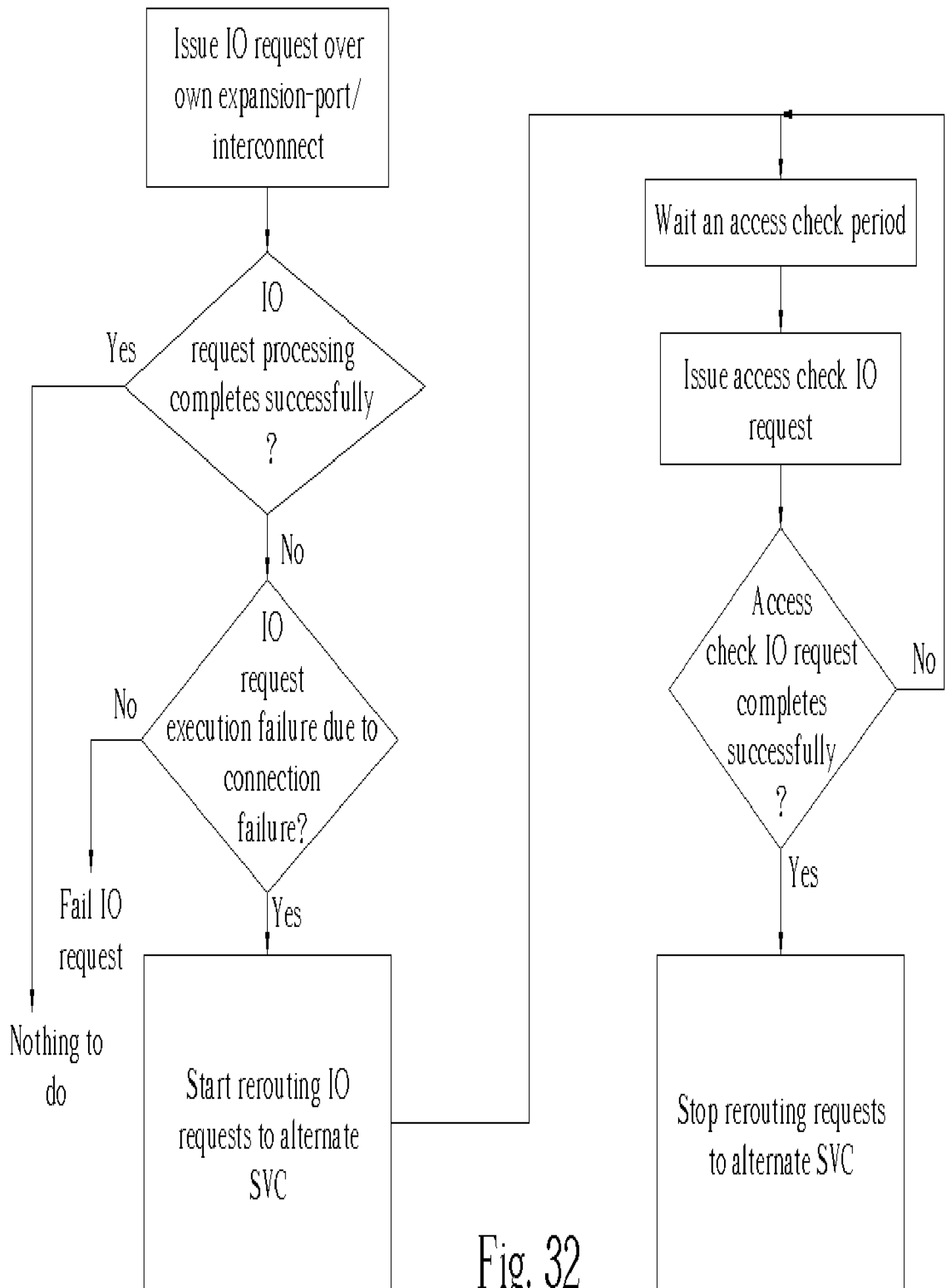


Fig. 32



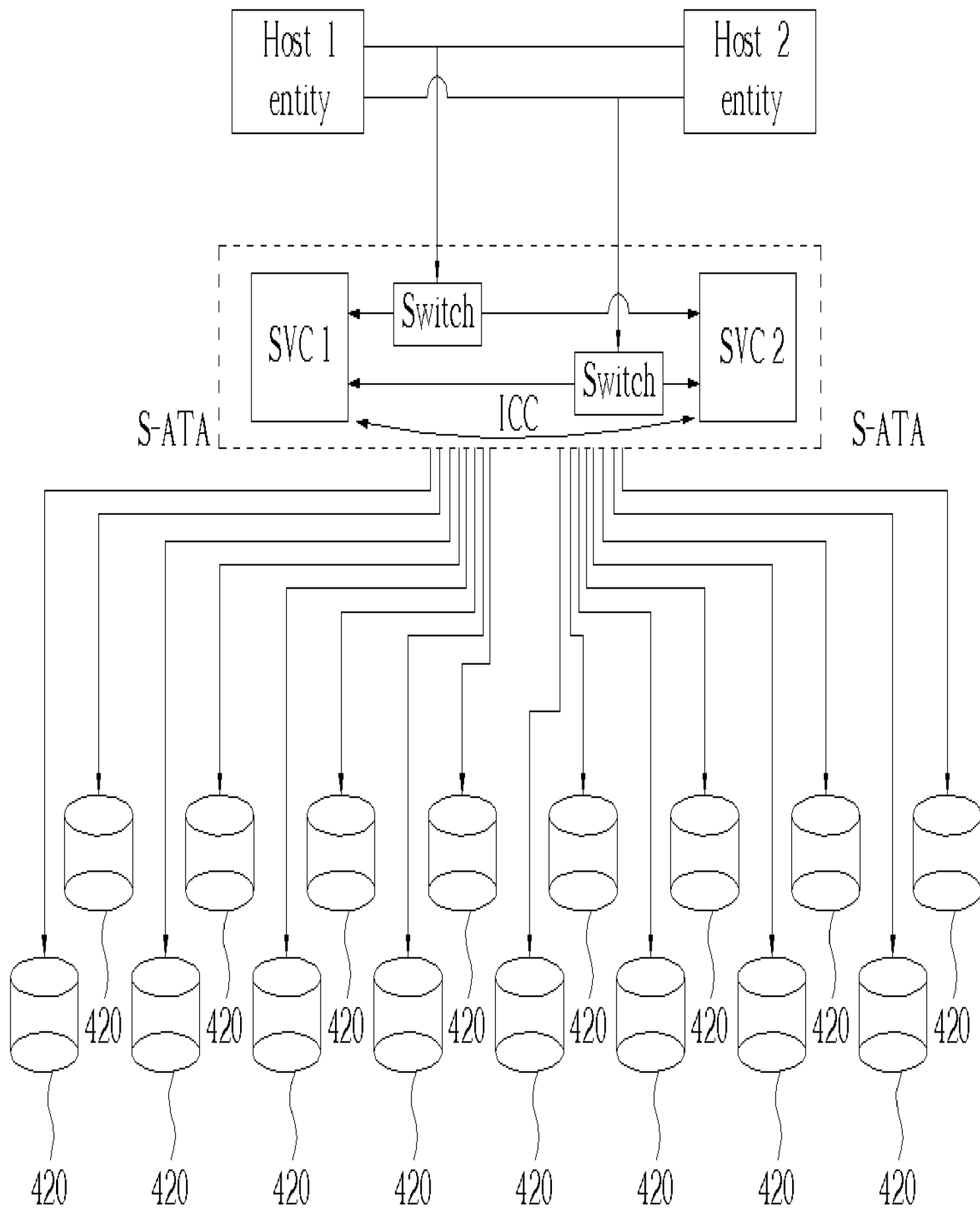


Fig. 33

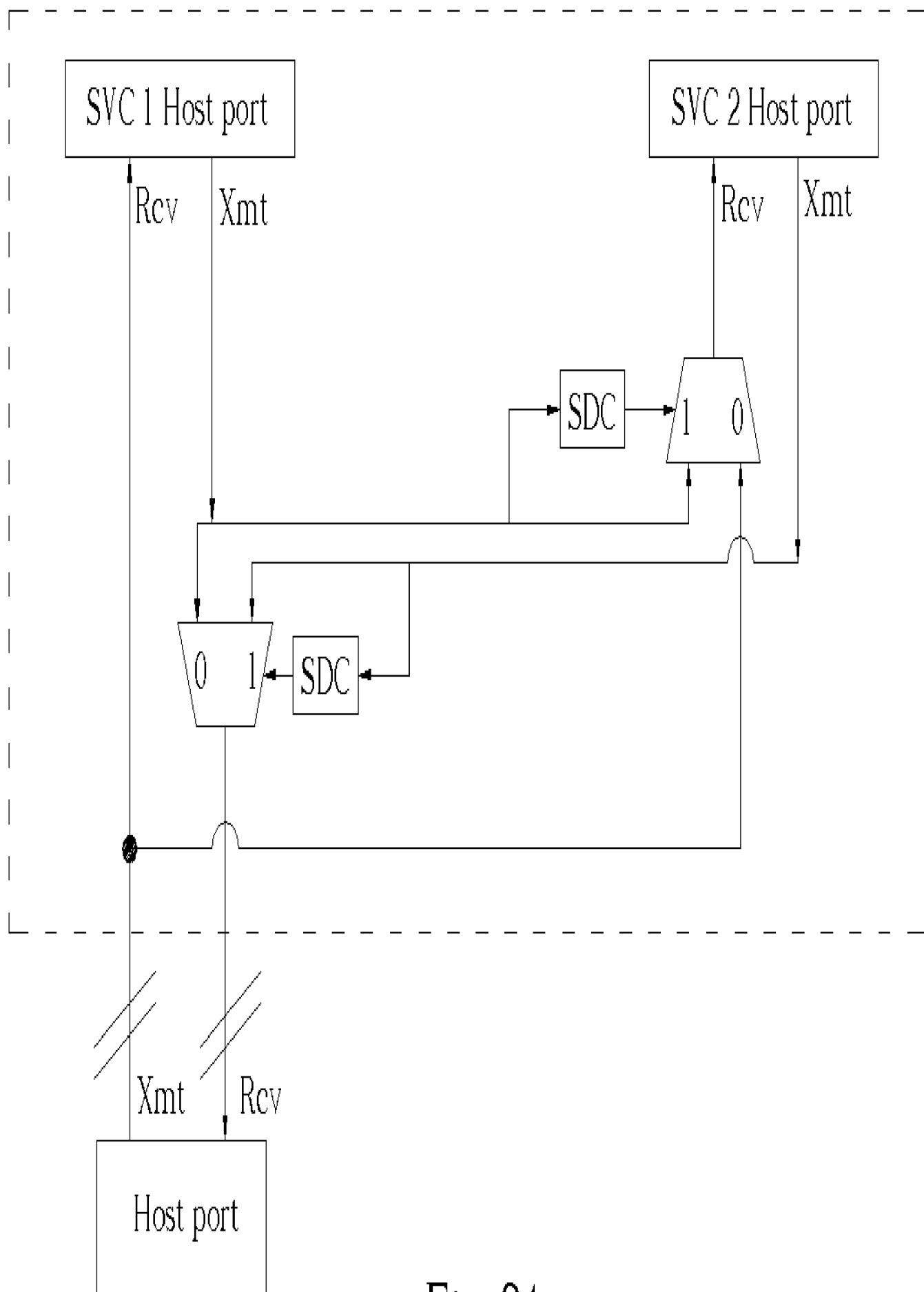


Fig. 34

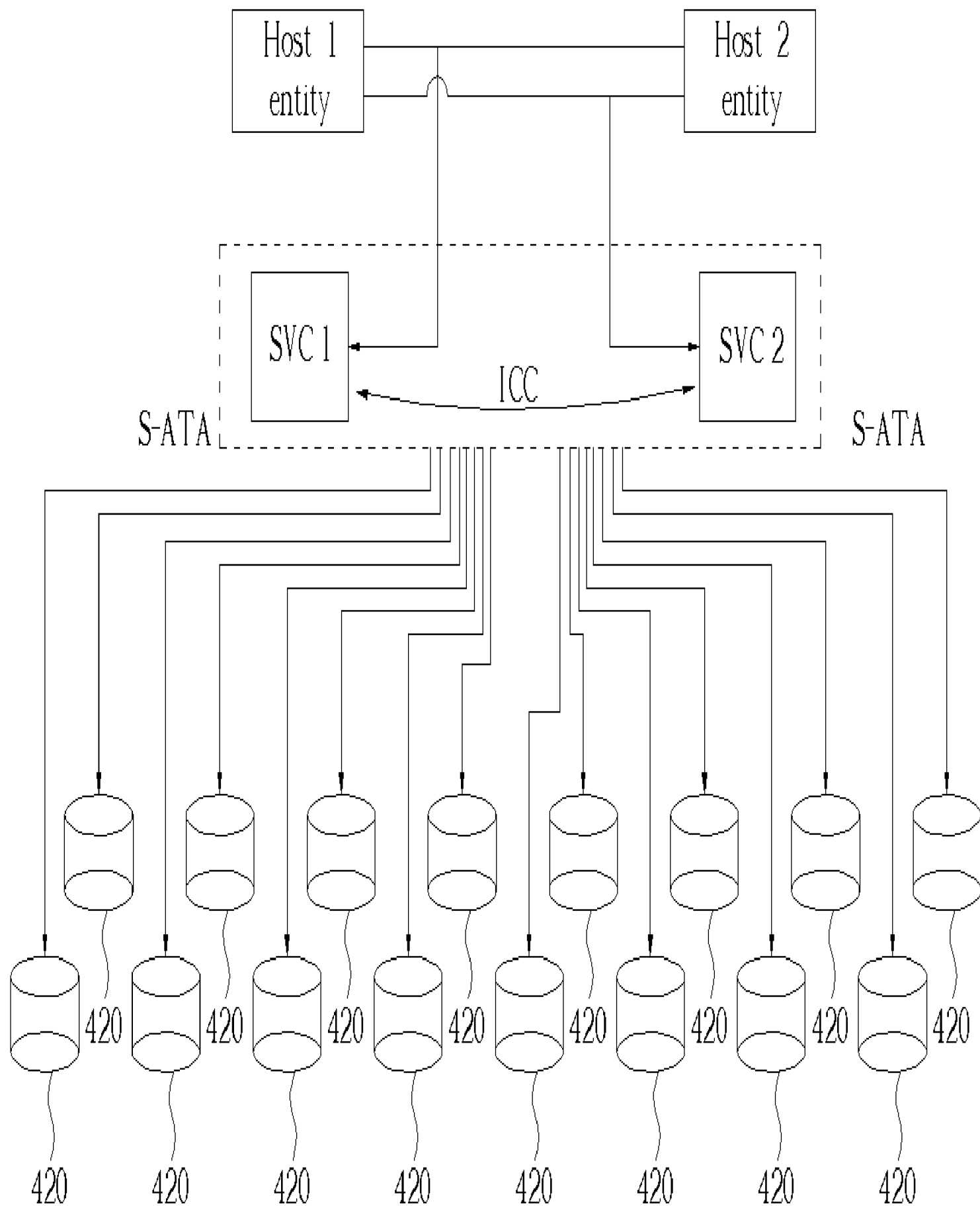


Fig. 35

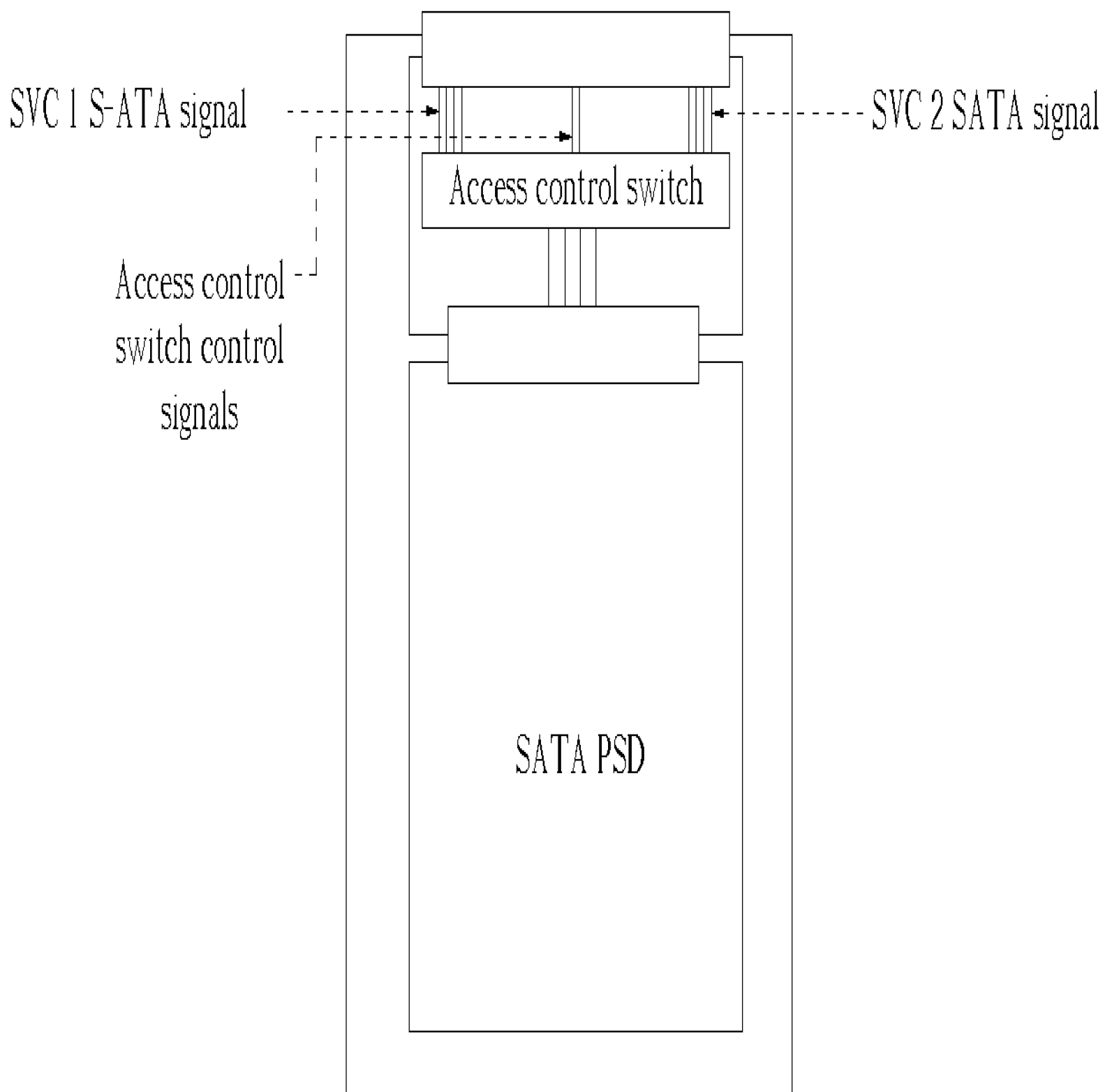


Fig. 36

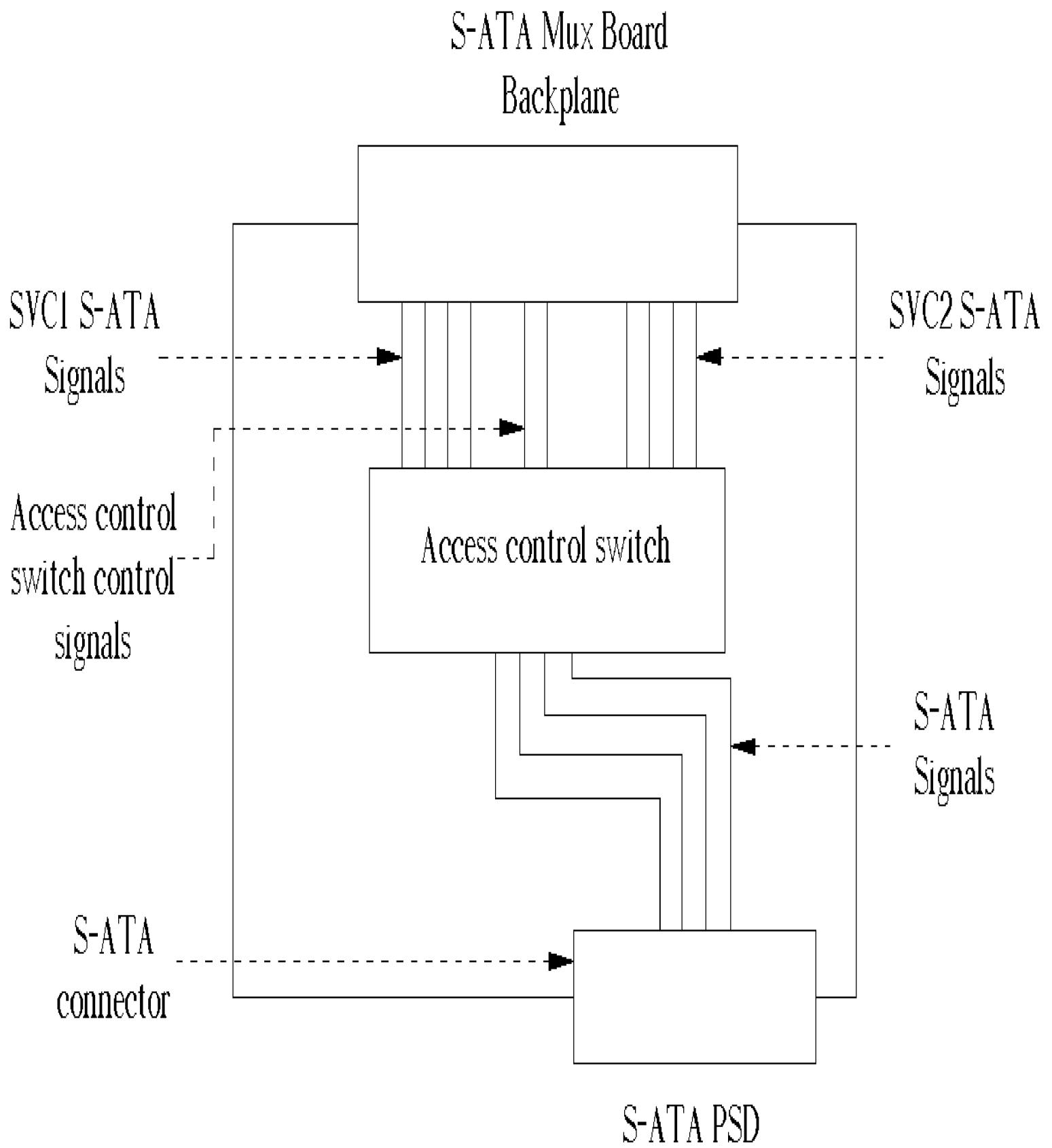


Fig. 37

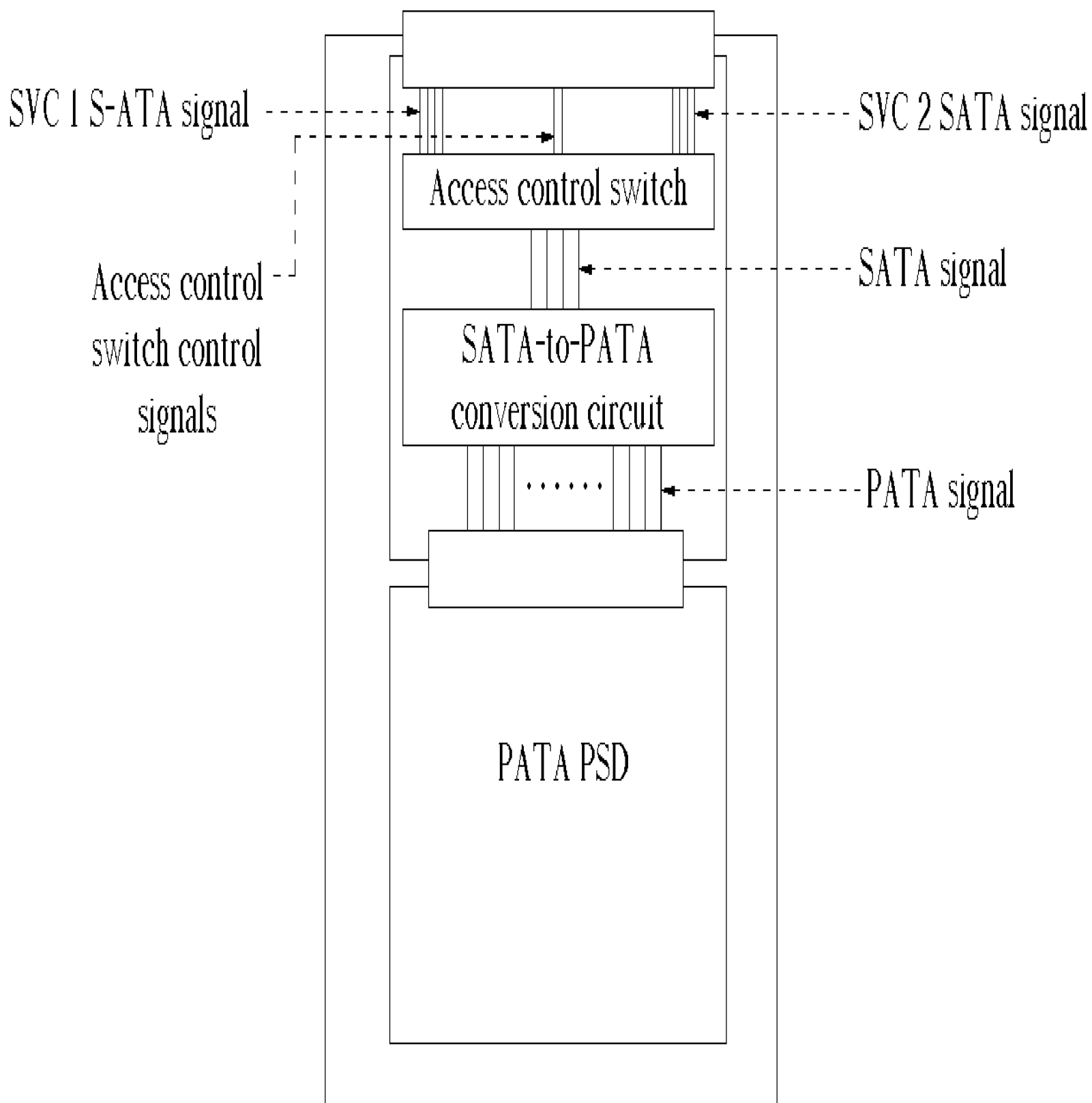


Fig. 38

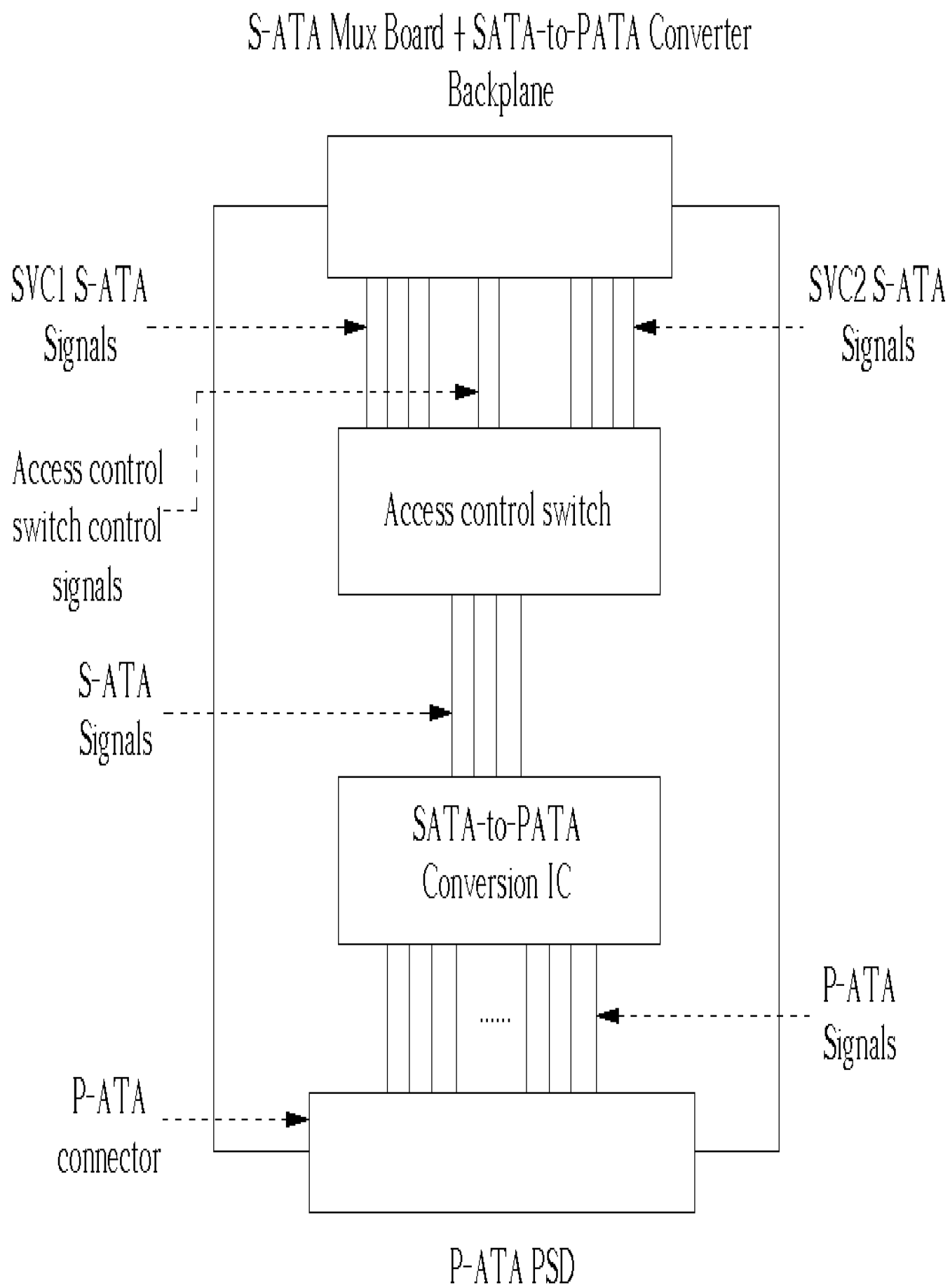


Fig. 39

CS1	CS2	CS	SI1->PI	SI2->PI
0	0	0	Closed	Open
0	Tri	0	Closed	Open
Tri	0	0	Closed	Open
Tri	Tri	1	Open	Closed

Fig. 40



CS1	CS2	SI1->PI	SI2->PI	Note
0	0	Undef	Undef	*:most recent changed one of CS1, CS2 gets access.
0	1	Open	Closed	
1	0	Closed	Open	
1	1	*Note	*Note	

Fig. 41

Loop Connections	M1	M2	M3	M4	M5
$C1 \Leftrightarrow P1, C2 \Leftrightarrow P2$	0	0	0	0	0
$C1 \Rightarrow C2 \Rightarrow P1 \Rightarrow C1$	1	1	0	DC	DC
$C1 \Rightarrow C2 \Rightarrow P2 \Rightarrow C1$	1	DC	1	0	0
$C1 \Leftrightarrow P1$	DC	0	0	DC	DC
$C1 \Leftrightarrow P2$	DC	DC	1	1	0
$C2 \Leftrightarrow P2$	0	DC	DC	0	0
$C2 \Leftrightarrow P1$	0	1	DC	DC	1

$C_n$ :  $SVC_n$ ,  $P_n$ : Storage Unit Port  $n$ ;  $n=1, 2$ .

Fig. 42

S1	S2	R1	R2	M1	M2	M3	M4	M5
Val	Val	0	0	0	0	0	0	0
Inv	Val	0	0	1	0	1	0	0
Val	Inv	0	0	1	1	0	0	1
Val	Val	1	0	0	0	0	1	0
Inv	Val	1	0	1	0	1	1	0
Val	Inv	1	0	1	0	0	1	1
Val	Val	0	1	0	0	0	0	0
Inv	Val	0	1	0	0	1	0	0
Val	Inv	0	1	0	1	0	0	1

Fig. 43

C1	C2	R1	R2	M1	M2	M3	M4	M5
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0
0	1	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1	0
1	0	1	0	1	0	1	1	0
0	1	1	0	1	0	0	1	1
0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	1	0	0
0	1	0	1	0	1	0	0	1

Fig. 44

S1/C	S2/C	R1	R2	M1	M2	M3	M4	M5
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0
0	1	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1	0
1	0	1	0	1	0	1	1	0
0	1	1	0	1	0	0	1	1
0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	1	0	0
0	1	0	1	0	1	0	0	1

Fig. 45